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MACROMODULAR
COMPUTER DESIGN
PART 1.
DEVELOPMENT OF MACROMODULES

VOLUME V
LABORATORY PERSONNEL AND BIBLIOGRAPHY

Technical Report No. 48

FINAL REPORT - FEBRUARY, 1974
CONTRACT SD-302 (ARPA)

COMPUTER SYSTEMS LABORATORY
WASHINGTON UNIVERSITY
ST. LOUIS, MISSOURI

MACROMODULAR COMPUTER DESIGN
FINAL REPORT - CONTRACT SD-302
FEBRUARY, 1974

Technical Report No. 48

PART 1 - DEVELOPMENT OF MACROMODULES
VOL. V - LABORATORY PERSONNEL AND BIBLIOGRAPHY

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The views and conclusions contained in this document are those of the authors and should not be interpreted as necessarily representing the official policies, either expressed or implied, of the Advanced Research Projects Agency or the U.S. Government.

Computer Systems Laboratory
Washington University
St. Louis, Missouri

ABSTRACT

This volume gives names and titles of all personnel associated with the Macromodular Computer Design project for the period March 29, 1965 through February 2, 1974, and references to project-supported or project-related publications for that period. The work was carried on within the Computer Research Laboratory of Washington University under the director of Professor William N. Papian until August 31, 1967. Following reorganization, the project has been carried on within the Computer Systems Laboratory, under the direction of Professor Wesley A. Clark until June 30, 1972; and subsequently under the director of Professor Charles E. Molnar.

Titles, authors, dates and abstracts of relevant Technical Reports and Technical Memoranda originating during this period are given, as well as a bibliography of related Washington University theses and dissertations and of publications in the open literature.

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1. PREFACE

This volume gives the names and titles of all personnel of the Computer Systems Laboratory for the period March 29, 1965 through February 2, 1974, and references to all supported or related publications for the period.

Titles, authors, dates and abstracts for Technical Reports and Technical Memoranda published by the Laboratory are given. Technical Reports are internally reviewed formal publications of the Laboratory, and are available from the Defense Documentation Center as reports supplied under ARPA Contract SD-302. Technical Memoranda are unreviewed internal publications of the Laboratory, and have served a variety of purposes including internal dissemination of information or proposed designs, recording of useful information for later reference, and providing instructions for use of specialized devices, programs, or systems within the Computer Systems Laboratory. Copies of some of these documents can be obtained by writing to the named author or to:

Director
Computer Systems Laboratory
Washington University
724 South Euclid Avenue
St. Louis, Mo. 63110

References to related theses and dissertations, and to outside publications such as books and journal articles, are also given.

Persons finding errors or omissions in these listings are requested to call them to our attention so that they may be corrected.

2. PERSONNEL

Professional Staff

Allmon, Allie M. -- Research Librarian
Anne, Antharvedi -- Research Engineer
Arnzen, Robert J. -- Research Engineer
Arthur, Randolph M. -- Research Associate
Ball, William E. -- Research Engineer
Barry, C. David -- Research Associate
Benso, Loretta M. -- Research Librarian
Berns, Robert I. -- Research Assistant
Bosshard, Heinz E. -- Research Associate
Bridger, David A. -- Programmer
Chaney, Thomas J. -- Research Engineer
Choi, Uisik -- Staff Engineer
Chou, C.K. -- Staff Engineer
Chuang, Ying Huang -- Research Engineer
Clark, Wesley A. -- Research Professor and CSL Director
Coaker, Christine D. -- Technical Writer
Cook, Robert A. -- Research Programmer
Dammkoehler, Richard A. -- Associate Professor
Dodds, Carolyn B.W. -- Research Programmer
Ellis, Robert A. -- Assistant Director
Franklin, Mark A. -- Research Associate
Fritsch, John M. -- Research Associate
Goblick, Thomas J., Jr. -- Associate Professor
Gottlieb, Margery G. -- Research Assistant
Graesser, Susan M. -- Research Programmer
Handler, Pablo M. -- Research Associate
Harada, Kazuaki -- Research Engineer
Jacobi, Thomas H. -- Research Associate
Johns, Gerald R. -- Assistant Director
Kane, Gerald R. -- Staff Engineer
Kline, Raymond M. -- Associate Professor
Koenig, Michael -- Research Engineer
Lewis, Howard C. -- Engineer
Little, Gerald R. -- Research Associate
Loeffel, Robert G. -- Research Engineer
Loughner, Gwenyth M.A. -- Research Librarian
MacCordy, Edward L. -- Administrative Officer
Marshall, Garland R. -- Research Associate
Mate, Levente L. -- Visiting Research Scientist
Matula, David W. -- Associate Professor
Mitchell, Barbara L. -- Research Programmer
Molnar, Charles E. -- Director
Newell, John A. -- Research Engineer
Noonan, John R. -- Staff Engineer
Olson, Richard E. -- Engineer
Oppenheim, Ronald W. -- Research Biologist
Ornstein, Severo M. -- Research Engineer
Papian, William N. -- Research Professor and CSL Director

Pepper, Maurice L. -- Research Engineer
Perry, Timothy C. -- Research Engineer
Pfeiffer, Russell R. -- Associate Professor
Pickard, William F. -- Associate Professor
Pinzuti, Jean Paul -- Engineer
Rabbat, Naguib B. -- Research Associate
Richardson, Archie D. -- Engineer
Rosenberger, Fred U. -- Research Engineer
Rothenberg, Stephen J. -- Research Engineer
Savage, Patricia B. -- Research Programmer
Simon, Richard M. -- Research Engineer
Snow, Laetitia H. -- Research Programmer
Stone, G. Oliver -- Engineer
Stucki, Mishell J. -- Assistant Director
Szejnwald, Henryk -- Staff Engineer
Thompson, Marvin J. -- Research Programmer
Towler, Joseph C., Jr. -- Audio-Visual Specialist
Wann, Donald F. -- Research Associate
Wilkes, Mary Allen -- Research Programmer
Zacher, Albert R. -- Research Engineer

Technical and Other Supporting Staff

Abbott, Robert A. -- Programmer
Arnold, Julie C. -- Programming Assistant
Auer, Roy Raymond -- Laboratory Assistant
Ballou, Carol B. -- Programming Assistant
Beitch, Janis J. -- Programming Assistant
Bibbs, Altha G. -- Laboratory Assistant
Bicket, Virginia L. -- Laboratory Assistant
Bickmore, Glen E. -- Technician
Bickmore, George L. -- Technician
Bing, Jean Ann -- Typist
Blatt, Stephen N. -- Research Assistant
Boggs, Lorraine C. -- Secretary
Boulware, Carol J. -- Technical Assistant
Branahl, Sandra B. -- Laboratory Assistant
Braselman, Arquilla E. -- Receptionist-Typist
Brinker, Gary S. -- Laboratory Assistant
Brodsky, Donna L. -- Receptionist-Typist
Bubb, John M. -- Draftsman
Case, Cynthia T. -- Research Assistant
Cely, Monte A. -- Laboratory Assistant
Chaney, Carol L. -- Typist
Chevalier, Robert L. -- Photographic Assistant
Clark, Bridgett R. -- Receptionist-Typist
Clayton, Sheryl A. -- Reference Librarian
Collins, Elisabetta W. -- Library Clerk
Cox, Ronald O. -- Project Technician
Davis, Caryn L. -- Clerk-Typist
Davis, Leila L. -- Clerk-Typist
Davis, Terry W. -- Laboratory Assistant

DeWoskin, Andrew T. -- Laboratory Assistant
Douglas, Bernice A. -- Secretary
Dubinsky, Janet L. -- Programmer
Duncan, Ida Lee -- Secretary
Durley, Chester A. -- Technician
Eby, Linda Lee -- Secretary
Fierst, Thomas C. -- Technician
Fox, Joanne E. -- Programming Assistant
Frankford, Carol S. -- Programming Aide
Friedman, Joseph -- Programming Assistant
Fries, Adelia L. -- Administrative Assistant
Gardiner, Cheryl D. -- Technical Typist
Gleason, Kenneth E., Jr. -- Technical Aide
Greenfield, James A. -- Engineer
Hallar, James C. -- Senior Technician
Hannaway, George W. -- Laboratory Assistant
Hollingsworth, Gerelyn P. -- Secretary and Technical Assistant
Hoog, Connie A. -- Documentation Specialist
Horstmann, Kathleen R. -- Laboratory Assistant
Hronek, James E. -- Laboratory Assistant
Irish, Dorothy -- Secretary
Johnson, David B. -- Staff Engineer
Joos, Robert J. -- Engineer
Kalish, Kathleen O. -- Receptionist
Kegin, Kathleen M. -- Receptionist
Kegin, Kevin M. -- Laboratory Aide
Keiper, Mary Ann -- Laboratory Assistant
Kelly, Mary Ann -- Secretary
Kinch, Norman T. -- Laboratory Operations Manager
Kohmar, Valerie A. -- Laboratory Assistant
Kuehn, Stephen J. -- Engineer
Kyle, Kevin R. -- Laboratory Aide
Lager, Edward C. -- Reference Room Trainee
Lane, Freddie F. -- Clerk-Typist
Langsam, Joseph A. -- Programming Aide
Lapin, Carol S. -- Programming Assistant
Latty, Doris -- Secretary
Laubenthal, N.A. -- Programming Assistant
Ledbetter, Edith D. -- Draftsman
Leeper, David G. -- Research Aide
Lewis, Christina J. -- Laboratory Assistant
Lewis, Kenneth W. -- Technician
Lewis, Larry W. -- Office Clerk
Lewis, Phillip L. -- Technician
Litzsinger, Janet K. -- Receptionist-Clerk-Typist
Martin, Renaud F. -- Technician
Maul, Janice K. -- Research Aide
Mayer, Nikolaus -- Project Machinist
McCurdy, John K. -- Engineering Assistant
Mehroff, Norma L. -- Executive Secretary
Mellinger, Michael J. -- Programmer
Meyer, George C. -- Shop Superintendent

Meyer, Robert W. -- Laboratory Assistant
Miller, Katherine R. -- Laboratory Assistant
Mills, Ronald -- Laboratory Assistant
Montwieler, Joyce H. -- Laboratory Assistant
Moore, Virtis E. -- Technician
Morris, Marilyn -- Secretary
Muckerman, Kathleen O. -- Clerk-Typist
Murrah, Michael -- Laboratory Assistant
Neumann, Geraldine M. -- Secretary
O'Brien, Martin W. -- Programming Aide
Osborne, Paul D. -- Research Aide
Owens, Donald H. -- Documentation Specialist
Pappas, Cathy S. -- Receptionist-Typist
Parker, Gary W. -- Project Photographer
Passero, Sharon Lea -- Receptionist
Patrick, Marsha G. -- Clerk
Pepper, Marianne B. -- Technical Assistant
Pummill, Walter H. -- Technical Writer
Rath, Kenneth F. -- Technician
Reed, Virginia R. -- Laboratory Aide
Risch, Craig O. -- Engineering Assistant
Robinson, G. Scott -- Technician
Rosenbloom, Elliot J., Jr. -- Technical Aide
Ruff, William A. -- Laboratory Assistant
Rung, Pamela J. -- Clerk-Typist
Sandel, David F. -- Laboratory Assistant
Sanders, Allen -- Laboratory Assistant
Schoepfle, Walter J. -- Programming Assistant
Schuetze, Stephen M. -- Staff Engineer
Shaw, Noel I. -- Programming Assistant
Shupe, David L. -- Project Photographer
Solovitz, Stephen M. -- Research Aide
Spence, James E. -- Technician
Stewart, David L. -- Project Assistant
Stewart, Sandra M. -- Technician
Stork, Judy M. -- Clerk
Swanson, Sylvia N. -- Library Trainee
Taylor, David T. -- Technician
Thake, Charles W. -- Chemical Technician
Thomas, Grady A. -- Technician
Towler, Constance F. -- Secretary
Wanek, Janice A. -- Laboratory Assistant
Wette, Hildegard C. -- Laboratory Assistant
Wilkins, Barbara J. -- Secretary
Williams, Elaine N. -- Technical Typist
Ziegler, Michael A. -- Machinist

Graduate Research Assistants

Abbott, Nadine A.
Baumrin, Judith A.
Bennett, Judith R.

Brown, Richard S.
Callaghan, John L.
Chen, Shang-Chun
Chen, Sam-Tung
Chen, Yuan K.
Cibulka, Lloyd
Couranz, George R.
Das, Santanu
Fang, Ting-Pien
Gilman, Alfred S.
Groll, Darin J.
Gomberg, David A.
Gralia, Mars J.
Gruendler, Edward P.
Guignon, John E.
Gupta, Ashok K.
Hruska, Milan
Hurtado, Marco
Inselberg, Armond J.
Jagadeesan, Muthuswami N.
Junginger, Gerhard E.
Kao, Chin-Chi
Keller, Robert M.
Kim, Duck-On
Kirby, Kathleen
Kitch, Donald C.
Lal, Jagdish R.
Lang, Paul D.
Liang, Kuo-Chee
Littlefield, Warren M.
Mack, Harold L.
Mallicoat, Samuel W.
Marasa, John D.
Matthews, John W.
Moses, Frederick
Niehaus, Carl A.
Olson, Andrew M.
Puccia, Charles J.
Ramakrishna, Venkatesiengar
Rawizza, Allan R.
Rubinfield, Louis P.
Seiden, Michael R.
Shah, Hasmukh R.
Shinn, Carl M.
Smith, Wendy C.
Srinivasan, Ramaswamy
Strom, Robert E.
Susarla, Sarma V.S.
Turner, Randall M.
Velten, David
Vemula, N. Rao
Vishnubhotla, Sarma R.
Wacker, William D.

Walton, Robert
Wang, Jen-yih
Wong, Kenneth F.
Wrenn, Richard F.

3. TECHNICAL REPORTS - TITLES AND ABSTRACTS

TR 1 2/66 A MACROMODULAR APPROACH TO COMPUTER DESIGN

Wesley A. Clark
Mishell J. Stucki
Severo M. Ornstein

Macromodules are proposed as a means to narrow the gap between computer system design and implementation. Use of these computer "building blocks" permits assembly of systems of any size or complexity while avoiding the ordinarily time-consuming and costly engineering. With primary objectives of flexibility and ease of use, macromodules can be a valuable experimental tool in the realization of new computer systems concepts.

TR 2 5/67 LAP6 HANDBOOK

Mary Allen Wilkes

LAP6 is an on-line program for the 2048-word LINC which uses the LINC keyboard and scope for communication with the user, and the magnetic tapes for storage and working area. It may be used for preparation and editing of any character string (manuscript) or specifically for LINC program preparation. For general manuscript preparation not all of section V and none of section VI will be of interest.

LAP6 handles the manuscript display in such a way that any portion of the manuscript can be displayed at any time and edited directly by simply adding or deleting lines. Changes are shown integrated with the manuscript display as the user types.

Meta commands provide automatic filing of manuscripts and programs on LINC tapes and handle the conversation and memory loading of LINC binary programs. Debugging aids include displays of symbol tables and errors, and repeatable access to the manuscript display for editing and reconverting. Meta commands may be added by the user to suit his needs.

The Handbook describes the "Standard" configuration of LAP6 when referring to specific tape block numbers or block areas (manuscript working area, file area, etc.). LAP6 may, however, have other configurations as described in the "Notes."

TR 3 7/67 THE DESIGN OF A TAPE MACROMODULE

Warren M. Littlefield

This report deals with the design and function of a Magnetic Tape System Module. The report indicates what is necessary to effectively utilize a LINC tape transport, and interface it to the computational world. The prototype was built out of MECL integrated logic used in the pulse mode.

TR 4 7/67 MACROMODULAR COMPUTER SYSTEMS

This report consists of reprints of a series of papers presented at the 1967 Spring Joint Computer Conference sponsored by the American Federation of Information Processing Societies at Atlantic City, April 19, 1967, as published in the Proceedings, Thompson Book Co., National Press Building, Washington, D.C. 2004.

TR 5 2/68 DEVELOPMENT OF AN ON-LINE IMAGE PROCESSING
SYSTEM FOR THE LINC

John E. Guignon, Jr.
Raymond M. Kline

The development of an on-line image processing system for the LINC (a small digital computer) is described with both hardware and software details being considered.

The purpose of the system is to operate on various types of optical images, endeavoring to process them so that a maximum amount of useful information is retrieved for final interpretation by the observer. Besides other processing techniques, contrast enhancement and subtraction have been implemented into the system to achieve this purpose. A mathematical model of the system is investigated and equations describing its capabilities are derived. Results showing several pictures before and after processing, as well as data verifying the mathematical model, are also presented.

TR 6 3/68 ANALYSIS OF IMPLEMENTATION ERRORS IN
DIGITAL COMPUTING SYSTEMS

Robert M. Keller
Donald F. Wann

This report discusses problems encountered with control networks in highly restructurable digital systems. In particular the treatment of implementation errors is covered with emphasis on concurrent processing. The implementation of concurrent processing networks may result in errors which will be quite complex to detect, and systematic methods are warranted. A model representing a particular type of computing system is presented, and methods for introducing concurrent control into the model discussed. The automatic detection of a certain class of errors caused by improper design of these systems is investigated. Graph theoretic representation is employed in demonstrating several error detection techniques. The properties of these techniques are compared and it is concluded that one technique of those investigated is of sufficient generality, thoroughness, and simplicity in implementation to be used for automatic error analysis.

TR 7 6/68 A UNIFIED APPROACH TO THE DESIGN AND USE
OF RESTRUCTURABLE COMPUTER SYSTEMS: THE
META MACROMODULE MACHINE

Robert A. Ellis

A restructurable computer system offers the user an evolutionary approach to the design and use of computer systems. To support this, a

TR 7 (continued)

unified approach is proposed in this report. A meta machine and its environment are described which provide the ability to treat a macromodular description of a system as a program to be executed or as a set of specifications from which the system may be directly implemented in macromodules.

TR 8 6/68 FLOS AND FLOD - SINGLE AND DOUBLE-PRECISION
 FLOATING-POINT PACKAGES FOR THE LINC

Charles E. Molnar

This report describes two related LINC subroutine packages for floating-point arithmetic. FLOS is a single-precision package written with speed and efficiency in the use of memory space as the principal objective. FLOD is a double-precision package which uses a similar number format and identical calling sequences. Both include subroutines for addition, subtraction, multiplication, division, fix, and float. Programs written to use FLOD can be run in single precision using FLOS with minimal changes.

(This Technical Report is no longer available; FLOS and FLOD have been replaced by FLOS-1R and FLOD-1R, described in TM 82).

TR 9 6/68 SAP: A MODEL FOR THE SYNTACTIC
 ANALYSIS OF PICTURES

Armond David Inselberg
Raymond M. Kline

A syntax-directed model is presented which is able to recognize and generate two-dimensional pictures while allowing a high degree of man/machine interaction. Starting with a field of points representing the picture, a string of symbols providing a structural description of the picture is produced by the syntactic component. The structural description, composed of higher level primitives (e.g., geometric symbols such as triangles and rectangles) and syntactic relations which exist between the primitives, is operated upon by the semantic component to provide a semantic interpretation for the picture. The syntactic component consists of a lexicon, a modified context-sensitive phrase structure grammar, and a set of transformation rules. The semantic component consists of a set of heuristics to abstract the picture and a modified context-sensitive phrase structure grammar which allows contextual restrictions to be applied to combinations of constituents existing at different levels of the syntax tree which syntactically describes the picture. Various aspects of the model have been programmed on the LINC (a small digital computer), the IBM 360/50, and the IBM 7072.

TR 10 10/68 A COMPUTER-DIRECTED SYSTEM FOR MEASURING
 DISTANCE BETWEEN EDGES IN OPTICAL IMAGES

Carl M. Shinn, Jr.
Raymond M. Kline

An automatic measuring system for time-varying optical images is described. After the operator specifies the location of the segment to be measured on an outline image produced by the system, the equipment

TR 10 (continued)

periodically prints the current length on a teletype. A detailed study of optical edge detection by two different transformations is given. Finally, tests of the system as a means of measuring and recording dynamic blood vessel diameters in the rat mesentery are explained.

TR 12 4/69 AN INVESTIGATION OF SOME EXTENSIONS OF A
METHOD FOR GENERATING POWER SERIES

Andrew M. Olson
William E. Ball

An exploration is carried out of various problems associated with extensions of a method for the computer generation of the power series solutions to differential equations. Among the problems considered are: 1) extending the error analysis to multidimensional series, 2) interpolatory and Laurent series expansions, 3) error analysis for Laurent series, and 4) the treatment of poles in the solutions.

TR 13 8/69 A DC TO DC CONVERTER FOR MACROMODULES

T. J. Chaney

This study examines single-ended and push-pull DC to DC converters to choose the type best suited to power central processor macromodules. The saturable base drive type of push-pull converter is chosen, after modification to compensate for possibly disastrous effects of current unbalance in the power transformer. An analysis and design procedure for this improved converter is given, and used to develop a 15-watt version. For macromodules requiring better voltage regulation, a modification of the single-ended type of converter is developed in some detail.

TR 14 9/69 CONTROL OF CONCURRENT OPERATIONS IN
ASYNCHRONOUS DIGITAL PROCESSES

F. U. Rosenberger
D. F. Wann

Methods are presented which can be used to analyze a sequential digital process and synthesize a process which performs the same operations but in less time by allowing concurrent execution of operations where possible. In the model used, concurrent execution of operations is controlled by branch operations which initiate concurrent paths of execution and by rendezvous operations which combine concurrent paths of execution after completion. Two types of errors which may occur in concurrent processes but not in sequential processes are distinguished. The first, called sequencing errors, cause the computed results to depend on the magnitude of the delays in the process operations and are due to operations being initiated before all of their data values are available. The second type of errors are called implementation errors and are caused by attempting to combine non-concurrent paths of execution with a rendezvous operation and by attempting to initiate an operation that is already being executed. The problem of detecting and correcting these errors is

TR 14 (continued)

eliminated by insuring that the synthesized concurrent process is free of sequencing and implementation errors. A precedence relation is determined for the operations of the process and is used to insure that no operation is executed until all operations whose execution must precede it are completed, thereby preventing sequencing errors. Dominance relations and directed cut sets, which specify the relationship between the execution of the operations, are used to avoid implementation errors.

TR 15 11/69 AN ANALYSIS OF BINARY CIRCUITS UNDER
MARGINAL TRIGGERING CONDITIONS

G. R. Couranz

Various methods for handling the asynchronous interaction of signals are investigated. The basic synchronizer circuit, used in many clocked systems, and the interlock, postulated to mediate control signal interaction in asynchronous systems, are shown to fail under certain realizable conditions. The failure is traced to flip flops used as state indicators in these control circuits.

The basic flip flop is modeled as a simple negative resistance device with load. Stable and semistable or metastable states are defined. The time required for the flip flop output voltage to stabilize after triggering is investigated. Large variations in switching time are observed when the trigger pulse drives the circuit operating point to the metastable point corresponding to the intersection of the circuit negative resistance region and the load line.

Circuit noise effects at and near the metastable point are investigated. Two methods for the solution of circuit equations, including noise effects, are developed. The first method employs Fast Fourier Transform techniques to determine circuit response to noise. The second method is a Monte Carlo simulation of circuit operation. A hard wired shift register random number generator, used in the simulation of the noise source, provides numbers at a rate that allows the computation of a large sample size.

Boundaries around the region in which circuit noise has significant effect are discussed. The probability that the circuit output voltage will be found in this region is computed for several sets of circuit parameters.

Simple flip flop circuits, using tunnel diodes for the negative resistance device, are constructed and tested. The probability that the output voltage has escaped the bounded region is determined and compared with the results obtained by solution of circuit equations. This comparison indicates that the results derived from solutions of circuit equations may be used to predict the flip flop's probability of reaching a stable state as a function of circuit constants and time.

TR 17 2/70 A FORMALIZATION OF FLOATING POINT NUMERIC
BASE CONVERSION

D. W. Matula

The process of converting arbitrary real numbers into a floating point format is formalized as a mapping of the reals into a specified subset of real numbers. The structure of this subset, the set of n significant digit base β floating point numbers, is analyzed and properties of conversion mappings are determined. For a restricted conversion mapping of the n significant digit base δ numbers to the m significant digit base numbers the one-to-one, onto, and order preserving properties of the mapping are summarized. Multiple conversions consisting of a composition of individual conversion mappings are investigated and some results on the invariant points of such compound conversions are presented. The hardware and software implications of these results with regards to establishing goals and standards for floating point formats and conversion procedures are considered.

TR 18 2/70 LAP6 USE OF THE STUCKI-ORNSTEIN
TEXT EDITING ALGORITHM

M. A. Wilkes

An algorithm which runs on a 2048-word LINC provides efficient on-line editing of character strings virtually unlimited in length. Fixed address LINC tape holds the character sequence in the manner of a scroll. Edited characters are spliced directly in or out of the scroll as it moves across a display scope under the viewer's control. A 512 character "playground" created at the splice point provides sufficient ease to permit changing the scroll contents dynamically, and thereby simplifies several problems commonly associated with on-line editing. Compensatory inserting and deleting are practical. Inserted characters require no special identification and scroll maintenance is automatic. Editing commands and editorial text identifiers are eliminated, and the number of characters which can be inserted anywhere is limited only by the length of the scroll. Line numbers, if provided, are resequenced automatically as the scroll contents change. As little as 2% of the scroll is manipulated in the memory at a time. Despite the relatively slow transfer characteristics of the tape, performance is satisfactory on a LINC for scrolls up to 23,040 characters and is not strongly dependent on the size of the playground.

TR 19 7/70 A LOGICAL DESIGN AUTOMATION UTILITY

Chin-chi Kao
Y. H. Chuang

Computer oriented algorithms for several laborious computations frequently encountered in switching theory and logic design are presented. They are algorithms for the computation of designation numbers, functional composition, detection of relations between Boolean functions, symbolic expansion of Boolean expressions, and approximate minimization of Boolean functions. These algorithms are useful in the construction of man/machine interactive systems for logic design automation. Machine independence and modularity are emphasized in the development of these algorithms. They have been programmed on the LINC computer.

TR 20 5/72 A MONTE CARLO COMPUTER FOR SOLUTION OF PARTIAL
DIFFERENTIAL EQUATIONS

Eitan Sadeh
Mark Franklin

The Discrete Monte Carlo methods for the solution of partial differential equations have been studied theoretically and experimentally. Several of the relevant algorithms were proved. A special purpose digital computer, the PDE machine, was designed and constructed from macromodules, and Monte Carlo solutions for illustrative problems were obtained. Error analysis has been made and experimental outcomes were compared with theoretical results. The PDE machine has been proved to be very efficient from the viewpoint of accuracy and speed in comparison to the general purpose digital computer.

TR 21 4/73 DATA AND CONTROL SIGNAL DISTRIBUTION IN A
MACROMODULAR DATA-PROCESSING MANIFOLD

John A. Newell

This report contains a brief functional description of each of the circuit elements employed by data-processing modules to generate, manipulate, or propagate control signals within a data-processing manifold. A block diagram of the control circuitry of each of the data-processing and storage modules is presented along with a detailed discussion of the control therein.

Control signal generation and propagation needed to accommodate the data transfers within and between data-processing manifolds is examined in detail. Word-length extension creates a special set of control requirements which are also discussed.

TR 22 1/72 AN AUTOMATED MEASUREMENT SYSTEM FOR MYELINATED
AXONS

Sarma V. Susarla
Raymond M. Kline

An automated system for performing measurements on objects in optical images is described. The system is specifically applied to the problem of obtaining the diameter histogram of myelinated axons from electron micrographs. Man-machine interaction is used for the identification of axons in the picture, while edge following and numerical integration techniques are employed in the measurement. Extensive data are presented showing performance characteristics of the system. Finally, an automated axon recognition algorithm of modest capabilities is described.

TR 23 4/73 MACROMODULAR SYSTEM DESIGN

Wesley A. Clark
Charles E. Molnar

Macromodules are "building blocks such as registers, adders, memories, control devices, etc., from which it is possible for the electronically naive to construct arbitrarily large and complex computers that work." In the seven years since this statement was made in the presentation of a program then being undertaken at Washington University, the design and construction of a several hundred unit macromodular inventory has been accomplished; and some 60 or 70 widely different "computers that work" have been constructed, used and dismantled. This report briefly reviews the operational aspects of this inventory and our experience in working with it, and illustrates some of our present attitudes and values concerning the macromodular approach, with special reference to biomedical research applications.

TR 24 5/73 VIDEO PROCESSING HARDWARE FOR USE WITH AN
IMAGE PROCESSING CAMERA

T. C. Perry

This paper presents the design of video processing hardware to best utilize an image dissector camera in an image processing environment. Although most of the work was done with the idea of using the results on a specific dissector camera, much of it is applicable to a wide range of photo-multiplier devices.

An analog integrator and digital timing circuit which measure the output current from an image dissector tube and produce constant signal to noise ratios of 10, 32 or 100 (selectable) are presented. A digital circuit which produces a number proportional to the log of the dissector current is also presented.

TR 25 2/74 A MACROMODULE USER'S MANUAL

Christine Dickson

This document serves as a comprehensive user's manual for macromodules. It supplies information on module capabilities and other facts needed in system design, and also gives the physical details necessary to the user in constructing and operating his system. Explanations are at the level of an "electronically naive" user, but some knowledge of machine-language programming is assumed.

TR 26 2/74 A USER'S GUIDE TO CHEMAST

Christine Dickson
C. David Barry
Robert A. Ellis
John M. Fritsch
Garland R. Marshall

CHEMAST (Chemistry Assistant) is a system of LINC programs for the modelling and display of small molecules from molecular formula input. This document is a comprehensive guide to the operation of CHEMAST. It explains the purpose and capabilities of the system, gives instructions for running the programs, and includes particulars on storage organization and on techniques for generation of molecular models.

4. TECHNICAL MEMORANDA - TITLES AND ABSTRACTS

TM 1 8/66 MACROMODULAR SIMULATION ON THE LINC

Carol Frankford
Robert A. Ellis

This report describes a set of macro instructions which may be used to simulate macromodular systems on the LINC. The essential characteristic of this scheme is that the user actually writes a LINC program (in macro form) to accomplish the simulation. Simulated modules may be partitioned into word lengths of any integer multiple of a LINC word. The number of modules that may be simulated is indefinite because of the ability to segment the simulation by the use of the LINC magnetic tape system.

TM 2 8/66 LINC L⁶

Carol Frankford
Robert A. Ellis

Based on the work of Kenneth C. Knowlton of Bell Laboratories, a list-processing language was developed for the LINC. Originally intended as an L⁶ translator, the LINC adaptation is so different from the original L⁶ that it cannot properly be called the same language. This report describes the structure and use of LINC L⁶.

TM 3 8/66 LIME (LINC MACRO EXPANDER)

Carol Frankford
Robert A. Ellis

This note describes a LINC macro expander program (LIME), which operates in conjunction with LAP5 to expand macro instructions into the appropriate sequence of individual LINC instructions. LIME accepts the text prepared by LAP5, and expands this text into a standard LAP5 manuscript which can then be converted by LAP5 routines.

TM 4 8/66 LIME OPERATING PROCEDURES

Carol Frankford
Robert A. Ellis

Operating procedures for LIME as described in Technical Memorandum No. 3.

TM 5 8/66 MACROMODULAR IMPLEMENTATION OF A FLOATING
POINT ARITHMETIC UNIT

D. F. Wann

Investigation of a complete macromodular floating point arithmetic unit having Floating Add, Floating Subtract, Floating Multiply, Floating

TM 5 (continued)

Divide and Normalize instructions is described. The number format consists of a 12-bit exponent in 1's complement notation, and all answers are returned in normalized form. Both serial and parallel control algorithms were investigated. Portions of the system were simulated on the LINC to check the algorithms. The complete system requires approximately 70 data modules and 90 control modules.

TM 6 9/66 SERIAL MACROMODULES

Robert A. Ellis

The design of a partial set of macromodules which operate by serial data processing techniques is presented. Detailed knowledge of the design of macromodules is assumed.

TM 7 9/66 A MACROMODULAR SYSTEMS SIMULATOR (MS2)

R. A. Dammkoehler

The MS2 control program and language enable an engineer or programmer to design macromodular systems and run programs on such systems simulated on a conventional digital computer. Input to the simulator consists of a standard set of function definitions for the basic macromodules, a description of the organization of the target machine, and data required by that program. Output from the present version of MS2 is an active level change map (a continuous trace of the internal control network of the target machine as it executes its program) and the results of computations performed by the target machine.

TM 8 10/66 UPDATING OF THE PRELIMINARY REPORT ON MACROMODULES

S. M. Ornstein

This memo is an INFORMAL updating of the Preliminary Report on Macromodules. Major changes include a switch from "freestanding" modules to a frame-like structure, with some accompanying changes in configuration. Also the modules have been separated into an electronics package with separable faceplate. Finally, the Data Validation scheme has been inverted to a Data Delivery Process.

TM 9 10/66 MACROMODULAR FACEPLATES

S. M. Ornstein

This memo proposes a set of faceplates for Macromodules. A suggested list of 11 basic types can be combined with inexpensive, colorful, labeled plastic overlays to form an adequate number of facades for all unit types and settings presently envisioned.

TM 10 12/66 THE GLITCH PHENOMENON

Warren Littlefield
Thomas Chaney

This paper defines a phenomenon which is inherent in all interactions between two asequential machines, and attempts to show how the problem may be solved with 100% reliability.

TM 15 12/66 ERROR ANALYSIS IN PARALLEL PROCESSING

Donald F. Wann

One of the main advantages of macromodular concept is the ability to quickly implement parallel oriented computer algorithms. It would appear that such construction will become increasingly important to the users and designers of macromodular systems and this memorandum is an initial attempt at listing, defining, and examining a few of the concepts and techniques of parallel processing. Two topics are considered: a) the mathematical restrictions imposed on parallel algorithms and b) the detection of implementation errors.

TM 16 2/67 A SYNTHESIS TECHNIQUE FOR A CLASS OF
TRANSITION LOGIC CIRCUITS

Ying Huang Chuang

An easy and systematic synthesis method for a large class of transition logic circuits is presented. The approach regards the circuit as a finite-state machine to avoid difficulties in asynchronous circuit design, yet without hazards or critical races. Circuits designed are constructed from several basic transition logic elements as well as ordinary gates.

TM 17 2/67 ARITHMETIC CONSIDERATIONS IN THE FUNCTIONAL
DESCRIPTION OF MACROMODULES

Mishell J. Stucki

It is proposed that the details peculiar to different number representations properly belong to that area of design called "irrelevant engineering details" and that they should therefore be removed, whenever possible, from explicit consideration of the user of macromodules. An approach for achieving this in the area of arithmetic operations is presented and discussed.

TM 18 1/67 TRAC IMPLEMENTATION OF MACROMODULAR FUNCTIONS

R. A. Dammkoehler
R. A. Cook
A. R. Rawizza

The TRAC definitions required for the simulation of macromodular systems utilizing coupled data modules are given. The number of 12-bit modules used to create an extended precision data module must be 9.

TM 20 4/67 PROBLEMS ENCOUNTERED WITH CONTROL NETWORKS IN
HIGHLY RESTRUCTURABLE DIGITAL SYSTEMS

D. F. Wann
R. A. Ellis

This paper discusses problems encountered with control networks in highly restructurable digital systems. In particular the treatment of implementation errors is covered with emphasis on concurrent processing. Concurrent processing may result in errors which will be quite complex to detect and systematic methods are warranted. Four meta control elements are employed in obtaining convenient concurrent structures. We analyze several error detecting schemes and conclude that the arc-node method with node partitioning appears to be the most realistic approach at this time. (Submitted to the First Annual IEEE Computer Conference, to be held September 6-8, 1967.)

TM 21 6/67 A CLOSED FORM SOLUTION FOR THE SYNTHESIS OF A
CLASS OF TRANSITION LOGIC CIRCUITS

Mishell J. Stucki

This paper presents a closed form solution for the synthesis of a class of transition logic circuits which includes most of the transition logic circuits used in present macromodular design. The paper does not include examples; it is presented as a foundation for future papers describing the specific circuits being used.

TM 23 6/67 FUNCTIONAL DESCRIPTION OF HYBRID MACROMODULES

D. F. Wann
R. A. Ellis

This memorandum describes the functional characteristics of ten hybrid macromodules that can be used for the processing of analog signals and for the synchronization of internal control operations. The emphasis is on modules that have both an analog and a digital parameter manipulation, while purely analog modules (such as integrators) are not considered. Several examples are presented illustrating the use of these modules.

TM 26 6/67 INTERLOCKEN

Warren Littlefield

This report introduces the concept of asequential machines, and the Interlock devices necessary to allow them to interact.

TM 28 6/67 A SURVEY OF SOME MACROMODULAR ENGINEERING PROBLEMS
AND PROPOSED SOLUTIONS

Asher Blum
Thomas Chaney
Richard Olson

A survey of the engineering work on the construction, communication, and power distribution of the macromodular system as of Spring, 1967, is presented. The coverage is qualitative and not too detailed.

TM 29 6/67 DESIGN DETAILS RELATING TO THE INTERCONNECTION OF
MECL I HARDWARE

Asher Blum

The problems of interconnection, for the purpose of transmitting signals, of macromodules designed with MECL I integrated circuits is treated in detail. Some of the thinking concerning system noise is discussed and design methods for the interconnection scheme currently in use are worked out. The report is intended as an initial effort at a designer's manual on the interconnection problem.

TM 31 7/67 RECOGNIZING BOUNDARIES OF MACROMODULAR CLUSTERS

Severo M. Ornstein

This memorandum discusses what seems to be a general method whereby a cluster of macromodules can recognize its own boundaries.

TM 32 7/67 IMPLEMENTATION OF TIME DEPENDENT ALGORITHMS IN
ASYNCHRONOUS COMPUTER SYSTEMS (OR, KEEP THE TIME, BABY!)

R. A. Ellis
D. F. Wann

This memorandum discusses the problems encountered when implementing time dependent algorithms on an asynchronous macromodular system. The use of a synchronizer element which will indicate "lateness" allows discrete program segments to be accurately initiated with a predetermined time relationship. A number of new macromodules are described, including a clock, delay, time clamp and clocked time clock. A buffer memory is presented and a technique derived for determining the required word size needed in data rate smoothing.

TM 34 8/67 CURRENT CONSUMPTION OF MECL II PRELIMINARY REPORT

Thomas J. Chaney

This document includes a table of current consumption values to be used for calculating power requirements of MECL II. Conclusions and caution statements are offered based on data taken on a small sample (257) of 8 different types of MECL II.

TM 35 8/67 MACROMODULAR DIVIDE

Patricia Brown Savage

This report described a division routine made of macromodules simulated on the LINC computer.

TM 36 8/67 A PROPOSAL ON INTERRUPTION AND PRIORITY
CONTROL SCHEMES

Kazauki Harada

On the assumption that a classical interrupt method would be used in the macromodular system, an interrupt control unit and an associated priority control unit were proposed. Next both units were modified to obtain the facility for various types of interrupt methods.

TM 37 9/67 REVISION OF THE LINE SENSING NETWORK

G. Oliver Stone

This is a detailed generalized derivation of the line sensing network. It supersedes all previous derivations because it takes the average MECL II input current into account. Also included is a brief about terminating mono-rail lines in their characteristic impedance.

TM 38 9/67 A MACROMODULAR FOURIER TRANSFORM COMPUTER

Charles A. Molnar

A preliminary design of a macromodular Fourier Transform computer has been carried out, using an algorithm of the "Fast Fourier Transform" type for the calculation. This memorandum is a preprint copy of a digest of a paper describing this design, to be presented at the Northeast Electronics Research and Engineering Meeting, November 1-3, 1967, in Boston.

TM 39 9/67 MACROMODULAR SINE, COSINE, AND MULTIPLICATION

Patricia Brown Savage

This report describes a sine and cosine routine made of macromodules simulated using the LINC. A calling function is included to illustrate referencing the macromodular sine and cosine. The cosine routine uses the sine as a subroutine and the sine routine uses a macromodular multiplication subroutine. Notes on the impressions and experiences of a new, electronically naive user appear as an addendum.

TM 40 9/67 CROSSTALK

G. Oliver Stone

This report examines crosstalk between electrically coupled lines. The crosstalk on printed circuit lines is considered in detail for the case of MECL II level changes.

TM 41 9/67 MULTIPLE ITERATIONS AND THE ARRANGEMENT OF CALL
ELEMENTS

Patricia Brown Savage

Notes on a possible algorithm for determining the number and optimal arrangement of call elements for more than four iterations of a sequence of operations. The algorithm is designed first to minimize the number of call elements and, after this criterion is met, to minimize the execution time.

TM 42 9/67 A MONTE CARLO METHOD FOR TESTING ASYNCHRONOUSLY
CONTROLLED CONCURRENT PROCESSES IN MACROMODULES

R. A. Ellis
Susan M. Graesser

This memorandum describes a LINC program which will find implementation errors in macromodular systems that employ concurrent processing. Input and output formats are discussed and illustrated with results obtained from several examples. This technique, while not elegant, currently represents the only available, automated method for this type of testing.

TM 43 10/67 A MACROMODULAR PROGRAMMING LANGUAGE (MACPL)

Donald Kitch
Robert Keller

MACPL is a programming language used to simulate macromodular computer systems on the IBM 360/50. The simulator is implemented using compile time macros in PL/1. The execution time of MACPL is 40 times faster than MS2.

TM 44 10/67 TIMING STUDY: TRANSFER LOGIC MODULES CONTAINING
THE UP-BUS

Mishell J. Stucki

It is proposed that the flip-flops in the register module be loaded by a pulse P which is turned on when the transfer signal arrives at the register and is turned off when the data delivery complete signal from the up-bus arrives at the register. Data delivery of the up-bus is to begin as soon as possible after the transfer signal arrives at the register, even if P is not yet turned on. To be considered are the timing constraints which must be imposed on the modules involved in the transfer process if the transfer process is to work properly.

TM 45 10/67 A SYNTACTIC AND CONTEXTUAL PATTERN RECOGNIZER:
A PRELIMINARY STUDY

Armond Inselberg
Raymond Kline

A model is presented which performs pattern recognition by syntactic and contextual analyses. The analyses are made on a syntactic string which represents a parsing of the graphic input. The present implementation assumes the parsed string as input and syntactically analyzes the parsing by abstraction, the use of a grammar, a discrimination net, and a test for contiguous constituents. The contextual analysis is executed by a set of heuristics and an inference making discrimination net.

The present research uses a set of geometric symbols as the primitives which compose various figures in out-door scenes. A syntactic graphic language is outlined which allows the user to create figures from the defined relations and primitives. Several examples are presented showing applications of this language.

TM 47 10/67 THE DESIGN OF A MACROMODULAR META MACHINE (M6)

Robert A. Ellis

This note presents the design of a macromodular meta machine. (M6). This computer, designed in terms of macromodules is capable of executing, in a program-like manner, a description of a macromodular system. In a sense, the M6 is described in its own machine language. The justification for the M6 has been developed elsewhere.

TM 50 10/67 PROGRESS REPORT ON MACKRO

Harold L. Mack

A macro-based, machine independent, assembly-language level language called MACKRO has been developed and is being implemented on the IBM 360/50. This paper formally defines MACKRO and describes the S360/50 implementation. MACKRO is meant as the target language for syntax-directed compilers which are not suited for generation of large amounts of code. In viewing a scale from high-level source language (for example ALGOL or FORTRAN) to the machine language object program which finally performs the data manipulations, MACKRO occurs at the point where machine dependence is introduced. Specifically, the translation of MACKRO is the final step to machine language, or to assembly language on the target machine. A machine independent representation for five data modes is used in connection with a three data-address instruction structure. Future work will deal with code optimization, both at the MACKRO source language level and at the object code level, and extension of the MACKRO assembler to a meta-assembler.

TM 51 1/68 ACCUMULATED CONVERSION ERROR IN A MULTI-COMPUTER
ENVIRONMENT

David W. Matula

A mathematical model for treating various existing kinds of computers as component computers of a multi-computer is described, and the incumbent problems created by non-standard data representation codes are considered. Major conversion difficulties are shown to exist when the numeric base for floating-point data differs in the various component computers. Floating-point "constants" which are successively converted as they are passed between the component computers become subjected to accumulated conversion error, thus suggesting new phenomena for numerical analysis.

Systems of floating-point numbers and rounding and truncation conversion mappings are mathematically characterized so that the problem of iterated conversions can be described in an abstract mathematical setting. When the different bases which occur in the component computers are all variants of a common base, (e.g., binary, octal, hexadecimal), it is shown that the accumulated conversion (relative) error is bounded and of the same order of magnitude as the possible errors of a single conversion on the least accurate component computer. However, when the bases involved are not variants of a common base (e.g., binary, decimal), it is shown that the conversion error for successive conversions of a constant can continue to grow, hence the value of a "constant" may drift far away from its initial value.

A general method is presented for controlling the growth of rounding conversion error by successive rounding reconversions back to a calculated standard floating-point format. Then an example is shown demonstrating that if one attempts to attain greater accuracy by carrying more digits in the standard floating-point format than our method specified, a greater accumulated error may be introduced.

TM 52 1/68 AN APPROACH TO THE SYNTAX-DIRECTED ANALYSIS OF
GRAPHIC DATA

Armond Inselberg

An approach is offered to the syntax-directed analysis of graphic data. A description of the nature of graphics includes a comparison of corresponding concepts in linguistics. The analysis, performed by a syntactic component, is described in terms of the grammars which comprise the components. Abstracting and contextual processing are related to similar processes in human pattern recognition.

TM 53 1/68 A CURRENT GUIDE TO MACROMODULAR SYSTEMS

Donald F. Wann

This memorandum reflects considerations relating to macromodules and macromodular systems and is an effort to summarize the present status of functional description. The items described include the frame, data and control modules, memory, cables and parameter plugs. In addition, comments on concurrent and multiple width operations, diagram preparation and generation of elementary operations are presented and inventory distributions for existing computer designs are tabulated. Since this report is a summary, a prior knowledge of macromodular concepts is assumed. It is the intent that this memorandum will periodically be revised as the macromodular effort proceeds.

TM 54 4/68 SINGLE BIT MANIPULATIONS WITH MACROMODULES

Donald F. Wann

This memorandum is concerned with the manipulations of single bit information within macromodular systems. The monitoring and modification of individual bits in a register are discussed as well as the treatment of isolated data bits such as when employing flags. Four new modules are proposed; flag, individual bit detector, individual bit set, and transfer register, and the usage of these modules are illustrated with several examples.

TM 55 2/68 AN UNLOCKED TWO-LINE INTERLOCK

George R. Couranz

In order to produce an interlock that is not dependent upon a clock and allowed a worst-case design approach, the energy concept is used to assign binary status. A basic design is developed, tested, and revised to produce a two-line interlock with a non-conflict channel selection time of 80 nsec.

TM 56 3/68 IDENTIFYING AND CONTROLLING CONCURRENT OPERATIONS IN
LOOP-FREE MACROMODULAR SYSTEMS

Fred Rosenberger

Methods are described to analyze a loop-free macromodular system with all operations performed concurrently. A technique is then described which can be used to synthesize an error-free control network for the system which will allow operations to be performed concurrently when possible. Although not all cases of possible concurrent operations are identified, the methods presented are effective for many cases.

TM 58 5/68 THE REVISED SIMPLEX MACHINE IMPLEMENTATION

Donald C. Kitch

The revised Simplex Machine was implemented by simulating the operations of the macromodular units using MACPL simulation language. MACPL is a MACromodular Programming Language to simulate the macromodular operations on the IBM 360/50.

TM 59 4/68 LINC IMPLEMENTATION OF A MINIMAL PATH FINDING ALGORITHM

Noel I. Keller

This report gives details on the implementation of a LINC program which finds the shortest path between two points in a maze. The algorithm of Lee (1) with modifications by Akers (2) was used. The program may be used with blockages in the maze specified by the user, and also in "compound" problems in which there are a number of sets of end-points, each set forming blockages for all other sets, and each path forming blockages for its successors.

TM 60 3/68 DIRECT UTILIZATION OF FLOWCHARTS TO REPRESENT MACROMODULAR SYSTEMS

Susan Graesser
Robert Ellis

This memo presents the initial step toward the direct utilization of a two-dimensional form of input to represent macromodular functions. The specific purpose of the program reported here is to transpose keyboard flowchart input into corresponding single dimension output derived directly from the morphology of the flowchart. In the future, this concept will be correlated with the several proposed notations for the representation of macromodular systems.

TM 61 5/68 BROADCAST INFORMATION PROCESSING SYSTEMS

W. A. Clark
C. E. Molnar

A potentially powerful means of organizing a computing system is to "broadcast" fixed programs or data from a central "transmitter" simultaneously to any number of "receivers" which carry out computations. The transmitter repeatedly broadcasts all of the information in its stored library, and only one-way communication from the transmitter to the receiver is required. The power of the scheme lies in the fact that the continuously available broadcast information makes it possible for large numbers of small receivers with limited local working storage to do very large and complex jobs at low cost. Possible applications of this technique include desk calculators, hospital intensive care monitoring, teaching machines, and laboratory computers.

TM 63 7/68 DIVERSIFIED INTERLOCK MODULE

Kazuaki Harada

The modules presented here deal with random arrival signals on "first-come, first served" basis. The flip-flops solving hazards and keeping a queue are arrayed in matrix form. A row-wise sub-group of the modules can be used as an expandable interlock. The module is also capable of controlling multi-intersections of data highways.

TM 65 8/68 SOME CONCEPTS RELATING TO THE ORGANIZATION OF BROADCAST PROCESSING RECEIVERS

Gerald R. Kane

The technique of broadcast processing represents a potentially valuable scheme for performing large and/or repetitive tasks with very simple hardware at the receiving end of a broadcast library. The purpose of this memorandum is to present some concepts essential to the operation of receivers under broadcast control and to illustrate by a specific example a broadcast processing receiver.

TM 69 9/68 A DISPLAY SUB-ASSEMBLY

J. A. Newell
D. F. Wann

A free-standing display sub-assembly which will accommodate one of several available display units is suggested. This is a first effort or work-horse design which will accept 10-bit positional data on the horizontal and vertical axes and 8-bit data for Z axis or intensity modulation.

Data and control cables are connected to an image in the frame from which data cables may be connected to the display sub-assembly. It is suggested that all operating voltages be supplied through a separate cable from the frame.

TM 70 9/68 PROPOSED ELECTRICAL DESIGN OF THE FRAME SECTION POWER PLATE FOR PHASE I MACROMODULAR SYSTEMS

T. J. Chaney

This report presents an electrical design for the frame vertical power plate. The proposed design consists of two copper busses to transmit the 55 VDC power with a small printed circuit board for the reference, protection, preset, frame detection, and AC power lines. The protection and preset lines are single lines which supply signals to all the modules in a single column of frame sections. The maximum voltage drop in the 55 VDC power bus, the detection scheme, and tendency of the preset and protection signal nets to oscillate are discussed.

TM 70 (continued)

A requirement that the protect and preset lines on the lateral channel board be at least 0.100" wide is presented.

TM 71 9/68 TWO MACROMODULAR DESIGN PROJECTS: AN ARITHMETIC
EXPRESSION INTERPRETER, AND A HASH-CODED SYMBOL TABLE

Barbara Mitchell
Julie Arnold

An algorithm to translate algebraic equations for arithmetic evaluation is implemented in the first of these two macromodular design projects. The second builds and searches a symbol table, where hash-code addresses computed from variable names of table entries and a random scatter storage technique is used to handle collisions.

TM 72 9/68 A MACROMODULAR IMPLEMENTATION OF THE PDP-5

M. L. Pepper

A description of the PDP-5 is presented along with faceplate control maps and a flowchart of the control logic.

TM 74 10/68 DESIGN OF BUFFER MEMORY (FIFO)

M. N. Jagadeesan

A First in-First out memory (FIFO) using MECL II circuitry has been designed and a prototype model built. The design and construction of a memory with this type of organization are relatively simple compared with random access memories, and very high operating speeds can be obtained. Worst-case design calculations predict a minimum operating speed of 13.3 million words per second, which can be increased to about 25 million words per second by more precise control of internal timing. The three word by four bit prototype confirms these calculated performance figures. Expansion of word length and number of words does not appreciably influence the performance that can be achieved, as data and control connections have small fanouts regardless of memory size.

TM 76 11/68 DIGITAL COMMUNICATION SYSTEMS FOR BROADCAST
INFORMATION PROCESSING

Richard Olson
David Velten

The problem of data transmission in a broadcast information processing system is considered. Various modulation schemes are examined and compared. A practical system using television equipment is described.

TM 79 2/69 A PROGRESS REPORT ON COMPUTER CLASSIFICATION OF
PRESYNAPTIC DISCHARGES

Pablo M. Handler

Progress is reported on the attempts made to classify presynaptic discharges recorded with extracellular microelectrodes on the antero-ventral cochlear nucleus (AVCN) of the cat. Several methods were employed, but the hard conditions of the problem prevented the output of significant results up to now. Some future ways worth pursuing are indicated.

This memorandum was written while the author was on an International Postdoctoral Research Fellowship granted by the Public Health Service of the Department of Health, Education, and Welfare, while on leave from the University of Uruguay.

TM 80 6/69 DISPLAY AND MANIPULATION IN THREE DIMENSIONS

C. D. Barry
R. A. Ellis
S. M. Graesser
G. R. Marshall

The desirability of dealing with a three dimensional dynamic format which appears to be psychologically optimal for information transfer between a graphical display and the viewer must be considered in terms of cost, both in software and hardware. Recent attempts at various schemes of implementation of such a format on a small computer (LINC) have resulted in the ability to display and manipulate in three dimensions with relatively small cost in terms of additional computational time, program size, and hardware facilities. The use of stereo presentation and general matrix transformation for rotation about any given axis have been implemented with several variations including different stereo algorithms, rotation by analog computer, and design of special hardware with restructurable digital computer components. Particular attention has been paid to optimizing the fixed point arithmetic used in view of the small word length (12 bits) and the necessity for quick computations in order to maintain the dynamic display.

TM 81 5/69 THE COMMON DATA BUS: A CONCEPT AND MACROMODULAR
IMPLEMENTATION

Harold L. Mack

The common Data Bus (CDB), a data-oriented communications concept for concurrent processes, is described as a subprocessor in a computer processor. A specific implementation of such a subprocessor using macromodular technology is followed by a cost analysis of the CDB subsystem in macromodular units. A processor utilizing a CDB subsystem is shown to be modular, and potentially achieves maximum local parallelism without special program preparation.

TM 82 6/69 FLOS-1R AND FLOD-1R, SINGLE- AND DOUBLE-PRECISION
FLOATING POINT PACKAGES FOR THE LINC

M. L. Pepper
C. E. Molnar

This report describes a revision to FLOD, a double-precision floating point package for the LINC. The present revision corrects an error in the Add routine, requires fewer memory locations, and is slightly faster than the original program. The functional description of FLOD-1R is exactly identical to that of the original program FLOD.

For simplicity and convenience, this report reproduces the entire text of Technical Report No. 8, with the minimal modifications required to describe accurately the revised program. Those portions of this report which differ from the original are designated by a vertical bar along the left edge of the paper.

Since the original report also described a matching single-precision floating point package, FLOS, this report also describes FLOS. Although FLOS has not been revised, it is given the revised name FLOS-1R in this report.

TM 83 8/69 AN INTEGER APPROACH TO FLOATING POINT OPERATIONS

John D. Marasa
David W. Matula

Floating point operations on digital computers inherently introduce, accumulate, and propagate round-off and truncation errors in the course of their execution. It is also widely known that integer arithmetic should be used as often as possible in an attempt to reduce such error in final results. To this end, we have written a package of four FORTRAN subroutines for S/360 that multiply and divide by adding and subtracting integers that correspond to logarithms, and that add and subtract also using integer format in a simulated log-antilog manner which will introduce some truncation error.

TM 84 7/69 AUTOMATIC EXPANSION OF BOOLEAN EXPRESSIONS

Y. H. Chuang
C. C. Kao

Computer algorithms for expanding any Boolean expression containing "and", "or", and "complement" operators into a sum-of-products form by applying DeMorgan's theorems, associative laws, and distributive laws are presented. These algorithms have been programmed on the LINC, and are useful in automatic simplification of Boolean functions.

TM 85 9/69 DECIMAL AND BINARY FLOATING POINT ARITHMETIC
ROUTINES FOR THE LINC

Janet Dubinsky

Described are three separate sets of floating point arithmetic routines for the LINC:

1. Single precision binary floating point, using FLOS-1R as a basis.
2. Double precision binary floating point, using FLOD-1R as a basis.
3. Variable precision decimal floating point which uses a binary-coded decimal representation.

The FLOD and FLOS systems are exactly parallel. They contain routines for add, subtract, multiply, divide, fix and float integer and fraction, square root, exponential and logarithms base two, e, and ten computed by an Hastings approximation and a Taylor series, arctangent, sine, cosine, reduction of a radian angle measure to within $\pm 2\pi$, binary floating point to decimal conversion, and decimal to binary floating point conversion. The decimal system contains routines for add, subtract, multiply, divide, and conversion between the floating point decimal formats.

TM 86 7/69 MOLGRAPH: A PROGRAM TO MANIPULATE AND DISPLAY
MOLECULAR MODELS

R. A. Ellis
S. M. Graesser
C. D. Barry
G. R. Marshall

The organization and use of the LINC program MOLGRAPH is described. The program permits either keyboard or program specified operators to control the manipulation and display of molecular models which have been generated by the program CHEMGEN.

TM 87 7/69 CHEMGEN: A PROGRAM FOR GENERATING A DESCRIPTION
OF A MOLECULAR MODEL

C. D. Barry
G. R. Marshall
W. Schoepfle
R. A. Ellis
S. M. Graesser

The organization and use of the LINC program CHEMGEN is described. CHEMGEN transforms a description of a molecule, which is in the form of a LAP6 manuscript, into a form which is suitable as input to the program MOLGRAPH. The transforms are specified by directories which may be changed by the user.

TM 88 4/69 A METHOD FOR COMPUTER SAMPLING OF FAST RISE TIME
WAVEFORMS

George R. Couranz
Richard E. Olson

This technical memorandum describes an interface between a sampling oscilloscope and the LINC or μ -LINC. This interface provides a means of entering waveforms with second or nanosecond rise times into the computer for processing.

TM 90 11/69 SPECIAL PURPOSE SHIFT REGISTER IMPLEMENTING $C_{n,r}$

K. Harada

A circuit choosing r elements out of n elements, i.e., implementing $C_{n,r}$, is presented. Each element is corresponded to each digit of a binary number. r "1"s representing r elements are put on the r right-most digits of an n -digit binary register and shifted to the left-most digits of the register bit by bit. The circuitry is controlled by transition logic.

TM 91 12/69 TWO DIMENSIONAL FAST FOURIER TRANSFORM (2DFFT)

M. N. Jagadeesan

An efficient algorithm for computing Fourier transforms of function of two variables is presented. This algorithm requires only $2N \log_2 N$ complex additions (complex additions include complex subtractions) and $N^2 \log_2 N - 2(N^2 - N)$ complex multiplications. This is a considerable saving over the brute force method of N^4 complex additions and complex multiplications. Moreover, this algorithm requires $2N+2$ storage locations only. A LINC program is included for functions with 16×16 points.

TM 92 1/70 A METHOD LISTING ALL POSSIBLE PERMUTATIONS BY
REFERRING HAMILTONIAN PATHS

K. Harada

A practical algorithm listing all possible permutations of n elements, P_n , is given. Letting each element correspond to a vertex of a non-oriented complete graph, all possible Hamiltonian circuits are generated. The Hamiltonian paths contained in these circuits present the permutations without duplication and omission.

TM 93 2/70 DISPLAY OF HANDWRITING CHINESE CHARACTERS

Kuo-chee Liang

A method of displaying Chinese characters on the LINC scope so they resemble handwritten characters. Each character is developed from a sequence of individual STROKES in the order it is handwritten. Execution of various STROKE subroutines is accomplished by decoding double-word inputs. A character is constructed from a block of double-words.

TM 94 3/70 A SEQUENTIAL PERMUTATION NETWORK WITH
AUTONOMOUS BEHAVIOR

Kazuaki Harada

An autonomous sequential switching network capable of permuting its n input lines to its n output lines in a sequential cyclic manner covering all $n!$ permutations is presented. The network is constructed in multiple cascades according to an algebraic expression of products of transpositions.

The switching element permutes its input pair to its output pair according to its internal state $(1, 0)$. The number of the switching elements is $\frac{1}{2}(n^2 - n)$. The procedure is also given for setting of the switching elements in the network according to any specified permutation matrix.

TM 95 3/70 AN INTRODUCTION TO BLS: THE BASIC LANGUAGE SYSTEM

Harold L. Mack

The BASIC Language System (BLS) adds another dimension to the capabilities of the LINC. The new dimension is the high level language BASIC [1]. Included in the high-level language benefits for the LINC are a) structured mathematical expressions of arbitrary complexity, b) numeric man-machine interactions with a simple set of directives, c) a floating point minimum-maximum number range of $[.10000000E-1023, .9999999E1023]$, and d) a set of symbolic run-time debugging aids. These benefits are integrated into a single system, the BASIC Language System.

TM 96 4/70 MOLECULAR MODELING WITH A SMALL COMPUTER: AN
INTRODUCTION AND RESULTS OF INITIAL USE

C. D. Barry
R. A. Ellis
S. M. Graesser
G. R. Marshall

This paper describes a computer system which permits the construction, manipulation and display of models of molecular structures. The system is readily accessible to the chemist in his laboratory because it has been implemented on a small, laboratory-oriented computer (LINC). Several specific uses of the system are also described.

TM 97 4/70 SYSTEM LEVEL DIAGNOSIS OF DIGITAL MACHINES BY
GRAPH THEORETICAL METHODS: A PRELIMINARY STUDY

V. Raghunadha Sarma

Methods to represent digital machines by directed graphs are presented. The study is mainly concerned with obtaining loop-free graphical structures from the original system, and the strategic test-point pairs is discussed. The concept of generating functions is discussed in relation to connectivity.

TM 98 5/70 CABLE SENSING WITH THE MC1035 DIFFERENTIAL AMPLIFIER

F. U. Rosenberger

The presence or absence of a cable transmitting differential MECL levels can be detected by using one section of an MC1035 differential amplifier as a receiver for one of the differential signals from the cable. The circuit detects the presence of logic levels or an open circuit on a differential input and functions as a differential line receiver if logic levels are present. With no connection to the input pins, both outputs of a 1035 differential amplifier will be high, and this condition can be tested for to indicate the absence of a cable. Thus, the presence or absence of a cable from which a data delivery return would be required can be detected without the need of additional pins or jumpers in the cable. Several precautions must be observed when using the MC1035 to prevent the three circuits within a package from interacting with each other through the internal bias network.

TM 99 5/70 FLOATING POINT ADD, SUBTRACT, MULTIPLY, AND DIVIDE
IMPLEMENTED WITH MACROMODULES

M. L. Pepper

Presented is an up-to-date implementation of a macromodular unit for floating point arithmetic operations. Included are discussions of the algorithms, number representation, errors, and modular structure. The unit requires a minimum of 61 data modules and 16 control modules.

TM 100 6/70 BASE PEDESTAL LOGIC STRUCTURE

T. J. Chaney

This document describes the electrical operation of the macromodular base pedestal at the logic concept level. The implementation of this logic concept is not covered in detail. The necessary interactions with the logic modules, the frame blocks, and the console are pointed out. The designers of logic modules which require power sequencing or warm-up periods and designers of consoles should be especially interested in this document.

TM 102 7/70 FEEDTHROUGH IN MECL CIRCUITS

F. U. Rosenberger

Logic level transitions of input signals to a MECL package may produce short pulses on the package output(s), although the logical description of the circuit predicts no such coupling. In some cases the amplitude of these feedthrough pulses may approach the normal logic swing. They are caused by capacitive coupling through portions of the circuits and also by the charge and discharge of some junction capacitances to ground. Feedthrough only causes problems when it is necessary to insure a stable transient-free output from a logic circuit despite changes on some of the inputs. This is not required for all logic circuits in a system but will almost certainly be a requirement on some of the circuits, particularly where sequential circuits are involved, since a short transient may change the state of a flip-flop. In applications where feedthrough may be a problem its amplitude can be controlled by restricting fan-in, using only "OR" outputs, and avoiding some particular circuits such as the MC1016 altogether.

TM 103 7/70 BLS USERS REFERENCE GUIDE

Harold L. Mack
Richard Brown

The BLS USERS Reference Guide contains detailed operating instructions for the compilation and execution of programs written in BASIC-L, a LINC variant of the high level language BASIC. In addition to operating instructions, a complete list of diagnostics generated by the compiler and the run processor is given. An understanding of LAP6 operating procedures and BASIC-L are assumed.

TM 104 8/70 GENERAL PURPOSE micro-LINC INTERFACE

J. A. Newell

A functional description of an expandable interface system is presented. Daisy chaining, device selection, and level translating circuitry are discussed. Schematics, wiring lists, and pictorial information lend an aura of practicality to this discussion.

TM 105 9/70 { MECL } WILL GET YOU IF YOU DON'T WATCH OUT
 { MOTOROLA }

F. U. Rosenberger

Feedthrough, noise margins and the connection of unused inputs may trap the unwary MECL II user. A discussion of each of these problems is presented here along with information on experience gained from testing and using MECL II circuits. A basic knowledge of the operation and characteristics of MECL II as discussed in Motorola's "Microelectronic Data Book" is assumed.

TM 106 10/70 TRANSIENT AND EQUILIBRIUM HEAT TRANSFER
CHARACTERISTICS OF DUAL IN-LINE MECL II PACKAGES

Robert Arnzen

This report deals with experimental studies of transient and steady state thermal characteristics of dual in-line 14 pin MECL II packages. Investigations were carried out in still air and well mixed environments. Temperature dependent electrical parameters are employed for chip temperature measurement. It is concluded that manufacturers' specifications of thermal resistance are very conservative and could possibly be 2 to 3 times the actual measured values.

TM 110 10/70 A PLI PROGRAM FOR THE MINIMIZATION OF SWITCHING
FUNCTIONS USING EXCLUSIVE OR GATES

M. Jagadeesan

A PLI program for the minimization of switching functions in mod-2 sum-of-products form (i.e., using EXCLUSIVE OR gates) is given in this report. This program can be used for functions of up to 5 variables with or without DON'T CARE terms. The necessary changes to be made in the program are indicated for changing the DCL statements for a different number of variables. A comparison of the solutions for an example by different procedures is given.

TM 111 10/70 PRINTED CIRCUIT
BOARD AND LOGIC CHECKING PROGRAMS

Tim C. Perry

This report describes the function and use of a series of programs developed to aid in the design of printed circuit boards. The programs described are: CHECK, MERGE, CIRCHK, JOIN AND MOTHER.

TM 112 11/70 FAULT DETECTION AND LOCATION
FOR COMBINATIONAL CIRCUITS OF MACROMODULES

V. Raghunadha Sarma

Finding detection patterns which serve as detection cover are explained using the path sensitizing technique. An illustration is given using these methods. A brief description about the construction of detection patterns is given for four Macromodules. A method to obtain fault location information from the obtained detection cover is described in detail. Conditions which a collection of patterns have to satisfy so that the obtainable fault location information may be complete are given. A detailed description of range analysis which makes location possible is given. The need to automate the method is emphasized and algorithms for that are given. The remaining problem to be solved in combinational circuit diagnosis is described.

TM 113 11/70 MACROMODULAR SYSTEM
GENERATING TREES

Kazuaki Harada
Uisik Choi

A macromodular system generating all trees of a given graph without duplication is presented. The function of the system consists of bitwise generation of all combinations of m^n where $n+1$ is number of vertices and m is number of edges, and the examination of the connectivity of the given subgraph with $n+1$ vertices and n edges. A subgraph is treated by m dimensional vectors whose components are edges and, or $n+1$ dimensional vector whose components are vertices. The computation is performed by bitwise logical operations among these vectors. I/O operation is implemented by LINC. Input data consists of incidence matrix, number of edges and number of vertices of a given graph. Edge numbers are printed for every tree generation. The number of modules is 96 except memory modules and 31 for the subsystem implementing m^n .

TM 114 2/71 PATH, LOGIC - DIAGNOSTIC PROGRAMS

C. C. Kao

Two LINC programs have been developed to assist the fault diagnosis of macromodules, particularly the Arithmetic unit, the Logic unit, and the Shift unit. Single stack to 0 or stack to 1 failure is assumed. The programs can be run on a classic LINC.

TM 115 12/70 MACROMODULAR SORTERS

Kazuaki Harada

First a basic sorting network for n data is constructed by using n registers, $3n-2$ loaders, $n-1$ comparators, and accompanied call and merge modules. The operating principle of the network is the recursive execution of comparison and exchange of adjacent data.

Second, using the sorting network for $n=4$ and applying Shell's merge-exchange method, a sorter which consists of 49 modules and a 2^{12} -word memory is presented. The sorter is capable of sorting 2^{12} data with 9 passes.

Third, based on the same sorting network for $n=4$, another sorter by 4-way merge is proposed. The sorter is composed of 69 modules including a 2^{12} -word memory, and can sort 2^{11} data with 6 passes.

TM 117 3/71 FAIL-SAFE LOGIC --
A SURVEY AND A NEW SYNTHESIS APPROACH

Santanu Das

In recent years, quite a few researchers have directed their attention to the design of "fail-safe logic systems". In this note some of these works are reviewed and a new method of synthesizing fail-safe building blocks from commonly available logic modules is discussed.

TM 118 3/71 OVERLAY LABELS

M. A. Wilkes

Sixty functions from ten modules have been supplied with preprinted labels for the overlays. Selecting the correct label is simplified by using its code and color.

TM 119 4/71 A PATH ANALYSIS APPROACH
TO THE DIAGNOSIS OF COMBINATIONAL CIRCUITS

Sarma R. Vishnubhotla
Ying Huang Chuang

A unified procedure to find test patterns for detection and location of stuck-at-type single faults in the combinational circuits is described. A reduction algorithm to obtain a minimal set of detection patterns, and a location algorithm to obtain complete location information obtainable by external observation, are presented. The circuit may consider AND, OR, NOT, NOR, NAND, EXCLUSIVE OR and LOGICAL EQUIVALENCE gates.

A basis for the article are the single and multidimensional path sensitization (1,2) and the graph theoretical path sensitization (1,2) and the graph theoretical approach for system diagnosis (3). The main parts of this work are the construction of sensitization functions and the path analysis table, and the development of the reduction and location algorithms. The procedure is illustrated in detail by two examples.

TM 120 5/71 MOLECULAR MODELING SYSTEM -1
(MMS-1)

R. A. Ellis
J. M. Fritsch
C. B. W. Dodds

The first macromodular system for molecular graphics is described and evaluated. The system consists of an 86 cell macromodular computer, an Evans and Sutherland LDS-1 line Drawing System and a μ LINC 300. Two polypeptide molecules, myoglobin and insulin, were displayed and studied using crystallographic coordinates as input.

TM 121 5/71 THE CASE FOR COPYRIGHT

M. A. Wilkes

Much of the material produced in the research environment is regarded as proprietary. Copyright offers a simple way of protecting such material. The case is made particularly for copyright protection of computer programs, but the elements of securing copyright are the same regardless of the subject matter. It is recommended that most laboratory publications be routinely copyrighted.

TM 122 6/71 THE MACROMODULAR LISP MACHINE

Peter Deutsch*

A description of a macromodular system roughly equivalent to PDP-1 LISP without I/O, i.e., a LISP interpreter plus a dozen or so primitive functions, is presented. The machine was designed, assembled, and tested during a one week visit by the author in March. Timing measurements showed that approximately 700 nsec per operation (excluding memory references) were required, resulting in a system which was a factor of 2 to 4 slower than compiled LISP on the PDP-10. It is believed that by exploiting local parallelism, using the function caller, and rearranging the manifolds, the system might be able to gain as much as a factor of 3 in speed.

TM 124 7/71 MACROMODULAR FFT COMPUTER

Tom Jacobi

A macromodular computer for performing Fast Fourier Transforms has been assembled and demonstrated. The number of complex 12-bit points transformed was any power of two up to $2^{12} = 4096$. The computer required 76 macromodules for the computation, plus an additional memory of 4096 12-bit words for sines and cosines. The computation time was .67 seconds for a 4096 word transform for an average of 27.3 μ seconds per complete butterfly operation, in which a complex point was called from memory, multiplied by a complex number, added to and subtracted from another complex point called from memory, and the results stored. By use of a few additional modules and some restructuring of control the butterfly time could be reduced to about 17 μ seconds, to provide a transform time of .42 seconds for 4096 12-bit-accuracy complex numbers.

TM 125 7/71 A MACROMODULAR HADAMARD TRANSFORM PROCESSOR

Mark A. Franklin

This document describes a Fast Hadamard Transform Algorithm and a macromodular implementation of that algorithm.

*The author is a member of the staff of the Palo Alto Research Center of the XEROX Corporation.

TM 126 7/71 PL-1 PROGRAMS TO CONSTRUCT FAULT DICTIONARY
FOR COMBINATIONAL CIRCUITS

Sarma R. Vishnubhotla

A PL-1 program is first given to construct the ranges of a set of test patterns. The user is assumed to have the patterns at hand. The program can be used to ensure whether a set of test patterns are capable of detecting all the single faults or not. Also the complete location information contained in the set of patterns can be obtained from the fault dictionary. Another program is presented next to give detection and location information for double faults. The limitations of the second program are discussed.

TM 127 8/71 A MACROMODULAR STACK MACHINE

Mars Gralia

An elementary general purpose stack computer was designed and constructed using 47 macromodules. A complete description of the machine is attempted.

TM 128 7/71 LINC TO MACROMODULE INTERFACE

Tim C. Perry

A functional description of a series of LINC to macromodule interfaces is presented. A front panel picture is included for clarification.

TM 129 8/71 MACROMODULE HARDWARE DEBUGGING AIDS

Fred U. Rosenberger

Two units are described which are useful for debugging macromodular systems. One is a mini-console which allows the user to monitor and control signals, and the other is a light box which allows the user to monitor the state of data outputs.

TM 132 9/71 THE JANC

Nadine A. Bicket

The JANC is a small macromodular computer, good for demonstration, that uses the LINC for input, for transmission of commands from the user, and for examination of registers. Features include a special display scope and a "Talk to LINC" (TTL) instruction that accepts input from one of four adjustable knobs on the LINC.

TM 133 9/71 AN ALGORITHM FOR THE MULTIPLE FAULT DIAGNOSIS
IN COMBINATIONAL CIRCUITS

Sarma R. Vishnubhotla

This article presents an algorithm to locate all the faults existing in a combinational circuit which is faulty. The user does not have to know the multiplicity of the faults.

TM 135 9/71 CHEMAST: A COMPUTER PROGRAM FOR MODELLING
MOLECULAR STRUCTURES

C. D. Barry
R. A. Ellis
S. M. Graesser
G. R. Marshall

This report describes a set of computer programs which permits the construction, manipulation and display of models of molecular structures. The system is readily accessible to the chemist in his laboratory because it has been implemented on a small, laboratory-oriented computer (LINC). Structure input is by a linear notation which is entered via a keyboard. Manipulation includes changes to the geometry of the structure. Display is on the computer's built-in scope and consists of drawing stereo images of a stick-figure representation of the molecule. During display, orientation of the model can be dynamically controlled by the user.

TM 136 9/71 SPECIAL FAST "MULTIPLY" HARDWARE
FOR MACROMODULAR SYSTEMS

R. A. Dammkoehler
L. E. Davis
D. A. Gomberg
M. J. Gralia

Three specially designed devices were fabricated to perform specific multiplications (shifts) in a Macromodular system. The specific functions are described so other designers may be aware of their capabilities.

TM 138 10/71 ORGANIC MOLECULAR MODELS BY COMPUTER

C. D. Barry
Robert A. Ellis
John M. Fritsch
Susan M. Graesser
Garland R. Marshall

This is the text of the presentation by J.M.F. at the 162nd National American Chemical Society Meeting (September 13, 1971, in Washington, D.C.). This presentation was part of the "Symposium on Computer Applications in Organic Chemistry," sponsored by the Division of Organic Chemistry. To ease

TM 138 (continued)

the formidable task of portraying Molecular Graphics in action, the discourse centered on a thirty-minute film ("CHEMAST & WORK IN PROGRESS" - print of September 9, 1971).

TM 139 10/71 THE ANALYSIS OF PROCESSING STRUCTURES

R. A. Dammkoehler
M. J. Gralia
L. E. Davis
D. A. Gomberg

This memorandum presents the results obtained with a new structural analysis algorithm and an interesting, if not necessarily general, result obtained in an effort to synthesize a sequence-error-free design for a maximally concurrent macromodular processor.

TM 140 10/71 IMPLICIT CONCURRENCY AND THE MARCH COMPUTER

M. J. Gralia
R. A. Dammkoehler
D. A. Gomberg
L. E. Davis

Flowgraphs can be used to represent the structure of a program during execution. Furthermore, there exists an algorithm which detects the implicit concurrency in a given flowgraph. A programmable, albeit general purpose, computer was designed explicitly to support the algorithm. An introduction to the problem and to the machine are given.

TM 141 3/72 COMRAD

D. A. Gomberg
R. A. Dammkoehler
L. E. Davis
M. J. Gralia

A hand optimized, concurrent processing implementation of the MARC macromodular computer is described.

TM 142 11/71 { MECL } STILL
 { MOTOROLA } WILL GET YOU IF YOU DON'T WATCH OUT

F. U. Rosenberger

The summary sheets from TM 105, " { MECL } WILL GET YOU IF YOU DON'T WATCH
 { MOTOROLA } OUT"
have been updated and reproduced here.

TM 143 12/71 A FEW WORDS ABOUT MACROMODULE FUNCTION CODES

M. L. Pepper

Some types of macromodules can execute up to sixteen different functions. Which function, is determined by the function code. How that code is determined is the subject of this memorandum.

TM 144 4/72 A PAIR OF COMPUTER-BASED MOLECULAR MODELLING
SYSTEMS

R. A. Ellis

Computer-based molecular modelling systems use the power of a computer and associated display equipment to display and manipulate models of molecular structures. Two such systems are discussed: CHEMAST (Chemistry Assistant) uses only a small, laboratory computer and provides modest modelling capacities and MMS (Macromodular Modelling System) uses specialized equipment to model large structures. Presented at the IEEE Computer Society "Islands of Applications" Conference. June 8-13, 1972, Tokyo, Japan.

TM 145 3/72 PERFORMANCE OF A CABLE TV SYSTEM FOR THE TRANSMISSION
OF DIGITAL DATA

Marco Hurtado

A theoretical study has been made on the performance of a cable TV system for the transmission of digital data. Either an envelope detector or a synchronous detector have been considered as part of the system to obtain a base-band waveform, on which a threshold detector will operate to decide on the type of digital symbol received. A comparison of the performance of the system with both types of waveform detectors is presented.

TM 146 1/72 A CASE FOR CARD-EDGE CONNECTORS

Robert Arnzen

A presentation of rationale, establishment of requirements, and report on preliminary experimental investigations regarding the use of card-edge connectors in macromodular systems.

TM 147 1/72 COMPUTER AIDED LEARNING OF THE WRITING OF CHINESE
CHARACTERS - A STROKE CODING TECHNIQUE

Y. H. Chuang
S. C. Chen

A simple computer system for aiding to learn and to drill the writing of Chinese characters is proposed. The hardware comprises a LINC and a graphical input device, the Graf Pen. A stroke coding technique based on least square polynomial approximation is also presented.

TM 148 1/72 MONITORING THE MARCH COMPUTER

M. J. Gralia
R. A. Dammkoehler
R. H. Greenfield

Improvement of any controllable system is predicated upon the existence of performance evaluation techniques. This note describes a few methods applicable to the hardware/software of the March Computer.

TM 149 2/72 ON THE SCHEDULING OF PROCESSORS

M. J. Gralia

Consider a job which consists of many tasks, and a computer organization which consists of several identical asynchronous, but cooperating, processing units. This note describes several methods of assigning the tasks to processors without violating the sequencing constraints among tasks.

TM 150 3/72 MACROMODULES AT WORK: A ROUGHLY CHRONOLOGICAL LIST OF SYSTEMS

Christine Dickson

A list of all the unique or substantially modified macromodular systems designed and constructed since a working inventory first became available in January, 1971. Gives for each system the approximate date of initial assembly, the approximate number of cells, a brief functional description, names of the principal investigators, and references to any pertinent technical memoranda. Additional information on a particular system may be available from the principal investigator (s) and/or from the author of this memorandum.

TM 151 3/72 D/A MACROMODULE

F. U. Rosenberger

The D/A Macromodule provides two $\pm 5V$ analog outputs, controlled from the up bus, and a $1 \mu s$ 5V intensify pulse that can be used to drive a CRT display. In a point plotting mode points can be displayed at about a 300KC rate on a Tektronix 602 monitor scope. The analog outputs can also be used for any other purpose requiring analog signals and they have a settling time of about $1 \mu s$.

TM 152 4/72 MACROMODULE CORE MEMORY TIMING CONSIDERATIONS

H. Lewis
D. Richardson

The following report is the result of an extensive analysis of the inherent timing constraints placed upon a Controller module, including the Block Transfer Controller, which may use the 4096 x 12 bit stackable core memory module.

TM 153 4/72 ASYNCHRONOUS SEQUENTIAL MACHINES WITH CONTROLLED
SECONDARY EXCITATION

Y. H. Chuang
Santanu Das

A new method for race-free synthesis of asynchronous sequential machines is proposed. The state variables are realized with standard D flip-flops which are selectively excited with an internally generated clock, only when a change of state is necessary. It is shown that this synthesis method is simpler than those using S-R or J-K flip-flops. Considerable amount of saving in logic is also achieved, as the selective clocking gives rise to a large number of "don't care" entries in the flow-table, and we can use the economical state assignments available for synchronous sequential circuits.

TM 155 4/72 A PATH ANALYSIS METHOD FOR THE DIAGNOSIS OF MULTIPLE
FAULTS IN COMBINATIONAL CIRCUITS

Sarma R. Vishnubhotla
Ying Huang Chuang

Given any combinational circuit made up of AND, NAND, OR, NOR, NOT gates, a procedure is given to construct sets of patterns which are proved to be sufficient to detect every detectable multiple fault caused by many single faults simultaneously. Based on this result a practical algorithm is developed so as to locate all constituent detectable faults in one or more experiments. The lengthy process of dictionary construction for multiple faults is avoided and the algorithm can locate any detectable multiple fault. Both redundant and irredundant circuits without topological constraints are considered for both detection and location.

TM 156 5/72 A USER'S GUIDE TO CHEMAST

Christine Dickson
C. David Barry
Robert A. Ellis
John M. Fritsch
Garland R. Marshall

CHEMAST (Chemistry Assistant) is a system of LINC programs for the modelling and display of small molecules from molecular formula input. This document is a comprehensive guide to the operation of CHEMAST. It explains the purpose and capabilities of the system, gives instructions for running the programs, and includes particulars on storage organization and molecule generation techniques.

TM 157 5/72 A NEW HAZARD DETECTION TECHNIQUE

Santanu Das
Ying Huang Chuang

A new method of hazard detection is discussed in this note. The method is conceptually very simple and lends itself to easy mechanization. It can detect static hazards due to both single and multiple input changes. It detects if there is a hazard involved in transition between two input states. Further, it pin-points all the variables with respect to which the hazard exists. Unlike most of the existing techniques, it does not require the unwieldy conversion from binary to ternary function.

TM 158 6/72 HIGH-LEVEL LOGIC MODULES: A QUALITATIVE COMPARISON

R. A. Ellis
M. A. Franklin

In recent years several developments have occurred which provide a digital system description/design level above that traditionally available with conventional logic design components. This paper considers two systems of high-level logic modules: macromodules (MMs) developed by Clark et al., and register transfer modules (RTMs) developed by Bell and Grason. A qualitative comparison of these two module systems is provided by contrasting the goals of the designers and presenting four case study designs using the two module sets.

TM 159 5/72 A MACROMODULE SHIFT REGISTER RANDOM NUMBER GENERATOR

Eitan Sadeh
Mark Franklin

This memorandum describes a shift register random number generator which was constructed out of macromodules. The random number generator generates a two bit random number every 1.2 μ s. The generator requires 18 macromodules and was used as part of a Monte Carlo machine for solution of certain partial differential equations. The memorandum first discussed the theory behind shift register random number generators and then considers a macromodule implementation.

TM 161 7/72 FAULT-TOLERANT DIGITAL SYSTEMS: A NEW APPROACH AND
COMPARATIVE STUDY

Santanu Das
Ying Huang Chuang

A new method of reliability improvement using N-fail-safe logic has been proposed in this note. It has been shown that our scheme is superior to other redundancy schemes considering both static and dynamic conditions.

A unique feature of our scheme is that it has two levels of reliability - the "correct" output reliability and the "safe" reliability. The safe output indicates a failure in the system, and can be used to initiate manual or automatic corrective measures.

TM 162 6/73 USER'S GUIDE TO PERFORMANCE TESTS FOR THE EVANS AND
SUTHERLAND DISPLAY SYSTEM

T. C. Perry
C. B. W. Dodds
Barbara Mitchell
Christine Dickson

This document is a reference to the series of performance tests and the set of general-purpose subroutines written for the Evans and Sutherland display system. Performance test design goals and the scope of the tests are explained in an introduction; then a section on each test program gives details of operation. Full descriptions of the subroutines are included, so that the user may write additional test programs as needed. Lists of E & S instructions and diagrams of system interconnections are also included for reference. A basic knowledge of system operation is assumed.

TM 163 6/72 CC1-CC2: DRAWING CHEMAST MOLECULES ON A CAL-COMP PLOTTER

Christine Dickson
Susan M. Graesser

This document describes a CHEMAST file program that will draw molecules on a Cal-Comp plotter. (The program is presently operable only on the super-LINC.) A full explanation and complete operating instructions for CHEMAST itself are given in TM 156, A User's Guide to CHEMAST. Operating instructions for the plotter are given in LD 83, Instructions for Using the Cal-Comp Plotter, and in the other references listed in the bibliography.

TM 164 4/73 COMPUTER SYSTEMS LAB. USER'S MANUAL FOR THE PDP-11/40

Barbara Mitchell
Gary Brandenberger

This manual explains a subset of rules for using the 11/40 DOS system at CSL, as planned in April, 1973. These instructions are valid for a PDP-11/40 with 16K of memory, a DECwriter as the system input device, DEC-tape, an RK11 disk, an RK11 bootstrap loader, a high speed paper tape reader and paper tape punch.

The methods explained for accomplishing given tasks are not necessarily unique or optimal. Any additions are welcomed.

TM 165 8/72 CHEMAST AND POLYNUCLEAR RING STRUCTURES

Andrew Feinberg

The problems of writing directories containing groups with polynuclear ring structures are explained, and a list of rules for obviating them is offered. A new indole ring exemplifies the rules. A new SPD1R4, containing the groups BIL, BO, FRO, and DO, incorporates the new ring.

TM 166 8/72 WAVES - A USER'S GUIDE

Janis Beitch

A LINC program to teach Fourier Analysis graphically. The program is mainly designed for the student who has had an introduction to Fourier Analysis, to give him a more concrete understanding of its basic concepts and properties. WAVES was developed at Computer Systems Laboratory, Washington University, St. Louis, Missouri.

TM 167 9/72 EXTENSIBLE MACHINE

Robert A. Ellis
Janis Beitch

An extensible machine is one which permits smooth expansion of the capabilities of a computer system through the addition of new functions in a uniform and consistent manner. Implementations with macromodules and with existing machines are described.

TM 168 11/72 ON THE SCHEDULING OF PROCESSORS

Mars J. Gralia

Consider a job which consists of many tasks, and a computer organization which consists of several identical asynchronous but cooperating processing units. This note describes several estimates of the minimum time required to process the entire job.

TM 169 9/73 CONTOUR DRAWING PROGRAMS

Thomas Jacobi

Two contour drawing programs are described in this report. The first of these was devised to draw electron density contours, and if applied to two three-dimensional arrays of experimentally determined densities, two intersecting sets of orthogonal contours are generated for a three-dimensional display. Because many individual sets of contours are desired in interpretation of X-ray diffraction data, this program has been automated so that after choice of contour level (threshold) and volume of interest, the program then generates and stores the desired contour data.

The second program described herein was developed for display of contours on Ramachandran Plots, in which energy of a molecule is shown as a function of two angles. In this program those points whose energy is less than a selected value are displayed, and a cursor is then used to choose the displayed areas about which contours are to be drawn. Because the angle coordinates are cyclic, all contours which encounter a boundary (0 or 2π) are automatically continued at the opposite boundary (2π or 0).

TM 171 9/72 THE TESTOR MODULE

Mishell J. Stucki

The testor module was designed to aid in the testing and debugging of other macromodules. The purpose of this report is to describe the logical function of the module and to provide a list of pin assignments.

TM 172 3/73 A MACROMODULE MATRIX INVERTER

Robert A. Ellis
Fall 1972 Class of EE 461

A 96-cell macromodular matrix inverter was designed and constructed as a class project by the Fall 1972 class of EE 461. The system performed matrix inversion by augmenting the original matrix by an identify matrix and performing a Gauss-Jordan elimination. The m-compatible Datacraft Scientific Arithmetic Unit was used to perform necessary arithmetic operations. The system inverted a 62 x 62 matrix in approximately three seconds.

TM 174 2/74 MACROMODULAR MODELING SYSTEM-4 (MMS-4)

R. A. Ellis
J. M. Fritsch
T. H. Jacobi
G. R. Marshall
C. D. Barry

This document describes, with diagrams and flowcharts, the hardware and software of the Macromodular Modeling System-4, a specialized graphics system presently tailored to the display of large molecular models and electron density contours. Although this is not meant to be a user's or programmer's guide, it provides more details of implementation than do the introductory papers [TMs 138, 144, 190].

TM 182 12/72 BURLESK: THE USE OF SYSTEMATIC CONFORMATIONAL SEARCHES
IN CHEMISTRY

H. E. Bosshard
C. D. Barry
J. M. Fritsch
R. A. Ellis
G. R. Marshall

In investigations of phenomena which are a function of the conformation of a molecule under study, the data are often fragmentary and insufficient to determine a unique conformation. The most rational approach is a

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systematic search in which one iterates the possible conformations available to the molecule and calculates the function of interest. This is then compared with the desired value to see if the conformation under consideration is acceptable.

The difficulty with this approach, in general, is that it is a computer problem of enormous magnitude due to the inordinate amounts of central processor time that an efficient search consumes. This predicates use of a small machine. BURLESK is a system developed for a small laboratory computer (PDP-12, micro LINC-300) designed for this task.

TM 184 2/73 DATACRAFT SCIENTIFIC ARITHMETIC UNIT USER'S GUIDE

Lou Rubinfeld

In order to provide for floating-point arithmetic in macromodular systems a Datacraft Scientific Arithmetic Unit (SAU) has been provided with an interface which makes the SAU macromodule compatible.

TM 185 3/73 A REPORT ON THE TESTING OF THE MULTIPLY MODULE

Mishell Stucki
David Stewart
Michael Mellinger

A description is given of the technique and results of the multiply macromodule testing.

TM 186 3/73 THE TRANLINE SYSTEM FOR TRANSMISSION LINE NETWORK
SIMULATION

James Greenfield

The Tranline System allows the simulation of networks composed of linear, lossless, distortionless transmission line segments and various lumped terminating components such as resistors and capacitors. The simulation is accomplished using the principle of time domain reflections of voltage and current variations at network discontinuities. The network is described by a LAP6 manuscript using a small simple set of instructions. The system operates on a 16K μ -LINC computer and the simulation output is presented as a display on the CRT.

TM 187 3/73 A LOGIC HAZARD DETECTION AND ELIMINATION METHOD

Levente L. Mate
Henry Y. H. Chuang
Santanu Das

This paper is concerned with the detection and elimination of static logic hazards due to single and multiple input changes. The method involves only simple manipulation of the Boolean expression corresponding to the

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logic network. It not only detects the existence of hazards and determines the variable sets with respect to which the hazards exist, but also, for each of these sets, pin-points the subcubes within which each input transition involving exactly the changes of all variables in the set produces the hazardous output. Further, it can determine the terms the absence of which from the expression cause the hazards. Thus, the hazard can be eliminated by including these terms in the expression. The theoretical foundation of the method is given first followed by an example illustrating the procedure and its effectiveness. The procedure is formulated into two different algorithms, one for saving time and the other for saving memory. They have been implemented in FORTRAN. A related result on prime implicant generation is also included.

TM 189 4/73 MATHEMATICAL STUDY ON THE EFFECT OF NOISE IN A NEGATIVE-RESISTANCE BISTABLE DEVICE

Marco Hurtado

Bistable circuits which present a negative-resistance region are considered. Using a simple linear model for the negative resistance region, a study of the effect of noise on the time at which stable points are reached, from a given initial condition is performed. The theory of diffusion processes is used in the main part of the work.

TM 190 5/73 A MACROMODULAR GRAPHICS SYSTEM FOR PROTEIN STRUCTURE RESEARCH

John M. Fritsch
Robert A. Ellis
Thomas H. Jacobi
Garland R. Marshall

A specialized graphics system has been developed for protein research; this system achieves real-time display and manipulation for line-segment models containing up to 4095 end points. The hardware consists of three components: 1) a collection of hardware subroutines assembled from digital computer building blocks called macromodules, 2) vector-matrix transformation and display equipment and 3) a small stored-program computer. This document provides a general description of the system (overall considerations, hardware, software, data structure, applications, et al.).

TM 191 6/73 INTERFACING THE PDP-11/40 WITH RESTRUCTURED MACROMODULES

Gerald C. Johns

The initial interface has four classes of data and control ports for communication between the 11/40 and restructured modules. The form and function of these ports will be described after a short presentation of background information about both the 11/40 and the new modules.

TM 193 6/73 DISASSEMBLY OF THE TI 980A ROM

Stephen M. Schuetze

This memorandum gives a reproduction and disassembly of the contents of the ROM in the TI 980A computer.

TM 194 7/73 FLATDIR - A TWO-DIMENSIONAL CHEMAST DIRECTORY

Barbara Mitchell
Christine Dickson

FLATDIR is a directory to be used with the CHEMGEN program in CHEMAST. It allows the user to generate a two-dimensional (rather than three-dimensional) structural diagram of a molecule, and includes all groups available in RNGDIR. FLATDIR was designed to prepare molecules for drawing on a Cal-Comp plotter with the CHEMAST file programs CCl and CC2.

TM 195 6/73 CHEMX2: A LINC PROGRAM FOR TEACHING ELEMENTARY CHEMISTRY

Christine Dickson

CHEMX2 is an interactive computer program designed to aid in teaching certain aspects of elementary chemistry by allowing the student to "build" molecules and ions with the aid of a CRT display scope. It runs on a micro-LINC 300 of 4K (4056) or more twelve-bit words.

TM 196 6/73 PDP-11/40 INSTALLATION NOTEBOOK

Michael J. Mellinger

This manual provides information regarding current software and hardware implementations of the laboratory's DEC PDP-11/40.

TM 197 6/73 PRELIMINARY SPECIFICATIONS FOR THE MULTILAYER P.C.
BOARD CHECKING PROGRAM

Michael J. Mellinger

Due to insufficient memory, it has been impossible to program the fairly sophisticated checks originally hoped for in the P.C. checking programs for use on the PDP-11/40.

Because of the imminent production of the first of the new modules, and to test some untried input formats, a simple version of future programs are being written.

This document describes techniques and specifications for these programs.

TM 198 6/73 DISASSEMBLY OF THE TI 980A SYSTEM LOADER FOR THE ASR33
TELETYPE

Stephen M. Schuetze

This memorandum gives a disassembly of the TI 980A computer system loader for the ASR33 Teletype.

TM 199 8/73 ON THE HYSTERESIS OF THE TTL CIRCUIT WITH TOTEM-POLE
OUTPUT

R. Srinivasan
T. J. Chaney

The existence of a hysteresis loop in the transfer characteristic of TTL Gates with "totem-pole" output is described. A detailed analytical procedure to evaluate the width of the hysteresis loop is explained. Further, a theoretical analysis is followed to prove that the loop gain of the circuit configuration exceeds unity which is the condition for regenerative action. Because of the existence of this behavior the output characteristics of some of the TTL NAND Gates with totem-pole output circuit show that these gates behave like Current-controlled Negative Resistance (CNR) devices.

TM 200 8/73 MANUSCRIPT TYPING PROGRAM

Lou Rubinfeld

This report explains the usage and control of two manuscript printing programs, one for usage with a Model 37 teletype and the other for the Data printer line printer. Both programs justify the lines of print in addition to providing special characters.

TM 201 8/73 THE MODIFIED BOOTH'S ALGORITHM

Lou Rubinfeld

An increase in speed of multiplication can be gained by examining more than one bit of the multiplier at a time. The modified Booth's algorithm is one means to increase the multiplication rate. The algorithm is described. A proof of its validity is given along with an interpretation of the results.

TM 203 9/73 TILINC

Stephen M. Schuetze

TILINC is a LINC Teletype-simulation program for the TI 980A computer. This Technical Memorandum contains a description of the operation of TILINC and the necessary instructions for using several of TI-supplied 980A programs.

TM 204 9/73 DETECTING THE COMPLETION OF OUTPUT-CABLE DATA DELIVERY
WHEN THE PRESENCE OF THE CABLE IS CONTEXT DEPENDENT

Mishell J. Stucki

This paper treats the design of a circuit for detecting the completion of output-cable data-delivery in applications where the presence of the cable is context dependent. The paper describes the delivery sequence, two methods of indicating delivery completion, and two schemes for detecting cable presence. It is shown that a hazard-free combinational circuit can be designed for either choice of completion indication and for either scheme of cable detection.

TM 206 9/73 NMS - NEURON MODELING SYSTEM

Barbara Mitchell

NMS displays three-dimensional line drawings of neurons. Several options are provided for various manipulations and for displaying cells in small groups, singly, or in groups of dendrites. NMS is an application for the Macromodular Modeling System. It is organized like the Molecular Modeling System and uses many of the same programs. The data for the cell description is created on another system with a computer-controlled microscope.

TM 207 1/74 A GUIDE TO MORE RELIABLE SYNCHRONIZER DESIGNS

Thomas J. Chaney

Computer synchronizer reliability can be compromised by a fundamental, relatively obscure, and difficult to pinpoint failure mechanism that is apparently not generally appreciated by system designers and users. As computer speeds have increased during the last few years this mechanism has begun to cause a significant number of computer system failures. The failure mechanism involves the inability of synchronizers to resolve conclusively in a fixed period of time which occurs first, the interrupt event or the system clock pulse. Synchronizers usually attempt to make this decision with a flip-flop, which may receive a marginal input for certain incoming signal timing relationships.

Examples of anomalous responses of simple flip-flops to such marginal input conditions are presented, along with an example of a commercially available integrated circuit synchronizer design that does not respond properly to some input conditions. Experimental data are included that can help the synchronizer designer to estimate the reliability of a design.

The heart of an arbiter circuit which allows both a short average throughput time and high reliability is shown. The use of this arbiter circuit, however, requires that the interacting processes stop while the arbitrating circuit is making its decision.

TM 208 1/74 A FLOPPY DISC PRIMER

Robert J. Arnzen

This report is intended to serve as a comparative and representative survey of "floppy disc" data storage devices presently available on the market today. In addition, personal observations regarding various systems and their mode of operation are presented.

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13. ABSTRACT This volume gives names and titles of all personnel associated with the Macromodular Computer Design project for the period March 29, 1965 through February 2, 1974, and references to project-supported or project-related publications for that period. The work was carried on within the Computer Research Laboratory of Washington University under the director of Professor William N. Papian until August 31, 1967. Following reorganization, the project has been carried on within the Computer Systems Laboratory, under the direction of Professor Wesley A. Clark until June 30, 1972; and subsequently under the director of Professor Charles E. Molnar. Titles, authors, dates and abstracts of relevant Technical Reports and Technical Memoranda originating during this period are given, as well as a bibliography of related Washington University theses and dissertations and of publications in the open literature.			

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