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MACROMODULAR
COMPUTER DESIGN
PART 2
MANUFACTURING DESCRIPTION

VOLUME V
LOGIC DRAWINGS

Technical Report No. 34

FINAL REPORT - FEBRUARY, 1974
CONTRACT SD-302 (ARPA)
COMPUTER SYSTEMS LABORATORY
WASHINGTON UNIVERSITY
ST. LOUIS, MISSOURI

MACROMODULAR COMPUTER DESIGN
FINAL REPORT - CONTRACT SD-302
FEBRUARY, 1974

Technical Report No. 34

PART 2 - MANUFACTURING DESCRIPTION
VOL.V - LOGIC DRAWINGS

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The views and conclusions contained in this document are those of the authors and should not be interpreted as necessarily representing the official policies, either expressed or implied, of the Advanced Research Projects Agency or the U.S. Government.

Computer Systems Laboratory
Washington University
St. Louis, Missouri

ABSTRACT

This volume contains the circuit diagrams for the vertical boards used in the macromodule electronic subassemblies.

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A GUIDE TO DRAWING CONVENTIONS

In the process of designing a circuit board, the logic drawing has been our principal piece of documentation up until the time that the production documents are generated. The drawings thus contain circuit diagrams, parts lists, component counts, and certain information that is useful at specific stages of the design process. About half of the drawings in this volume are original logic drawings. The other drawings are revisions that no longer contain obsolete information or information to be found elsewhere. The revisions also have an improved notational form. In the text that follows, we first treat the conventions common to all of the drawings in this volume, and then treat the conventions peculiar to specific subsets of the drawings.

1. LOGIC FUNCTION SYMBOLOGY

The logic function symbology conforms in general to MIL-STD-806B. The principal exceptions are as follow:

A) Function Identification Only two tagging lines are used. The top line locates the function on the circuit board and the bottom line identifies the hardware. Most logic hardware used in the modules is Motorola's MECL II series. This logic hardware is identified by an M followed by two digits. The M is an abbreviation for MCL2 so that a tag such as M47 identifies the element as an MCL247. When there is also a letter suffix, e.g. M47B, the suffix indicates that the hardware is tested to standards other than those specified by Motorola. For more information on that, see the section on IC Testing. When hardware is not MECL II series, the bottom tag line contains the manufacturer's own designation number.

B) Interconnected Outputs The outputs of MECL II circuits can be tied together to implement the AND and OR functions, a feature which has been used extensively in the design of the modules. When outputs are tied together, the interconnection point is high if one or more of the outputs are high (the OR function) and is low if all outputs are low (the AND function). In the circuit diagrams, the interconnection point is generally not enveloped by a logic symbol. The symbols have been omitted in order to reduce the overall density of logic symbols and thereby make the drawings easier to read.

2. OTHER CONVENTIONS --- ALL DRAWINGS

A) The symbols used for components such as resistors, capacitors, diodes, etc., are industry standards. Each of these items is identified by a single tag line. In most cases, one must refer to the parts list for the circuit board in order to get any information about these components. This is only partly true for resistors, however. Resistors are tagged by an R followed by three digits. If the digit immediately following the R is listed in the table below, then the value of the resistor can be found from the table. If the digit is not in the table, then one must refer to the parts list.

<u>Digit</u>	<u>Resistor Value In Ohms</u>
0	zero (a jumper)
1	1500
2	750
3	121
4	15K
5	57.6
6	130

B) Connector terminals for signals entering and leaving the circuit board are represented by ovals. Tags internal to the ovals identify the terminals.

C) A small triangle with no internal tag represents a connection to -5.2 volts. This voltage is V_{EE} for MECL II circuits.

D) When MECL II logic functions are shown with inputs tied to -5.2 volts, the device behaves as if those inputs were tied to a logic low.

E) On some circuit boards, a few of the integrated circuits have unused logic elements. These elements are shown on the diagrams in a group unto themselves.

3. DRAWINGS 200.9D3 THROUGH 210.2D3

These are revisions of the original logic drawings. Obsolete information and information now found elsewhere has been eliminated. The circuit diagrams have been revised in an attempt to make them easier to understand and follow. They have the following features:

A) The elements of the diagram are arranged so as to minimize the number of long lines, minimize the number of interconnecting lines, and accentuate functional groupings. In a few instances, tie-points are used to eliminate long lines that could not be comfortably eliminated by other means. See 3D for an explanation of tie-point notation.

B) Certain functional groupings are enclosed in boxes and labeled to indicate the functions performed by the groupings.

C) Signals entering and leaving the circuit board are identified by two tag lines. One tag gives the name of the signal while the other tag, always in parentheses, indicates the significance of a logic high or low. (See 3E for a special case.) The polarity-indicating tag is subject to the following rules:

1. If the signal is a data bit, the polarity representing the data value 1 is indicated. The possible tags are

(1-L) and (1-H).

2. If the signal is a condition, the polarity representing assertion of the condition is indicated. The possible tags are

(A-L) and (A-H).

3. If the signal is a transition signal, the preset polarity of the signal is indicated. The possible tags are

(P-L) and (P-H).

D) Two forms of tie-point notation have been used. The more commonly occurring form employs a triangle (flag) containing a letter tag. The rule is that all identically flagged points on a diagram are interconnected. The other form of tie-point notation occurs only on drawing 203.2D3. A tie-point source is identified by a small arrow which is usually perpendicular to a line and pointing away from it. The number of destinations is indicated by a digit near the arrow. If the line to which the arrow is affixed is not already named, a name is given at the head of the arrow. A tie-point destination is identified by a logic function input connected to a tag. This tag is either the signal name of the tie-point source or the complement (NOT) of it. The assertion polarity (or value 1 polarity) for this tag agrees with the assertion polarity of the input to which it is connected.

E) On drawings 205.2D3 and 210.2D3 there is a pair of inputs whose second tagging line is "(A-NC)." The possible states for these inputs are NC (no connection) and ground (zero volts).

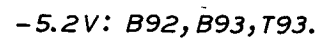
4. DRAWINGS 211.3D3 THROUGH 218.4D3

A) A small circle on a line (with a tag beginning with an H or a LH) specifies a plated-through-hole into which a component is not inserted.

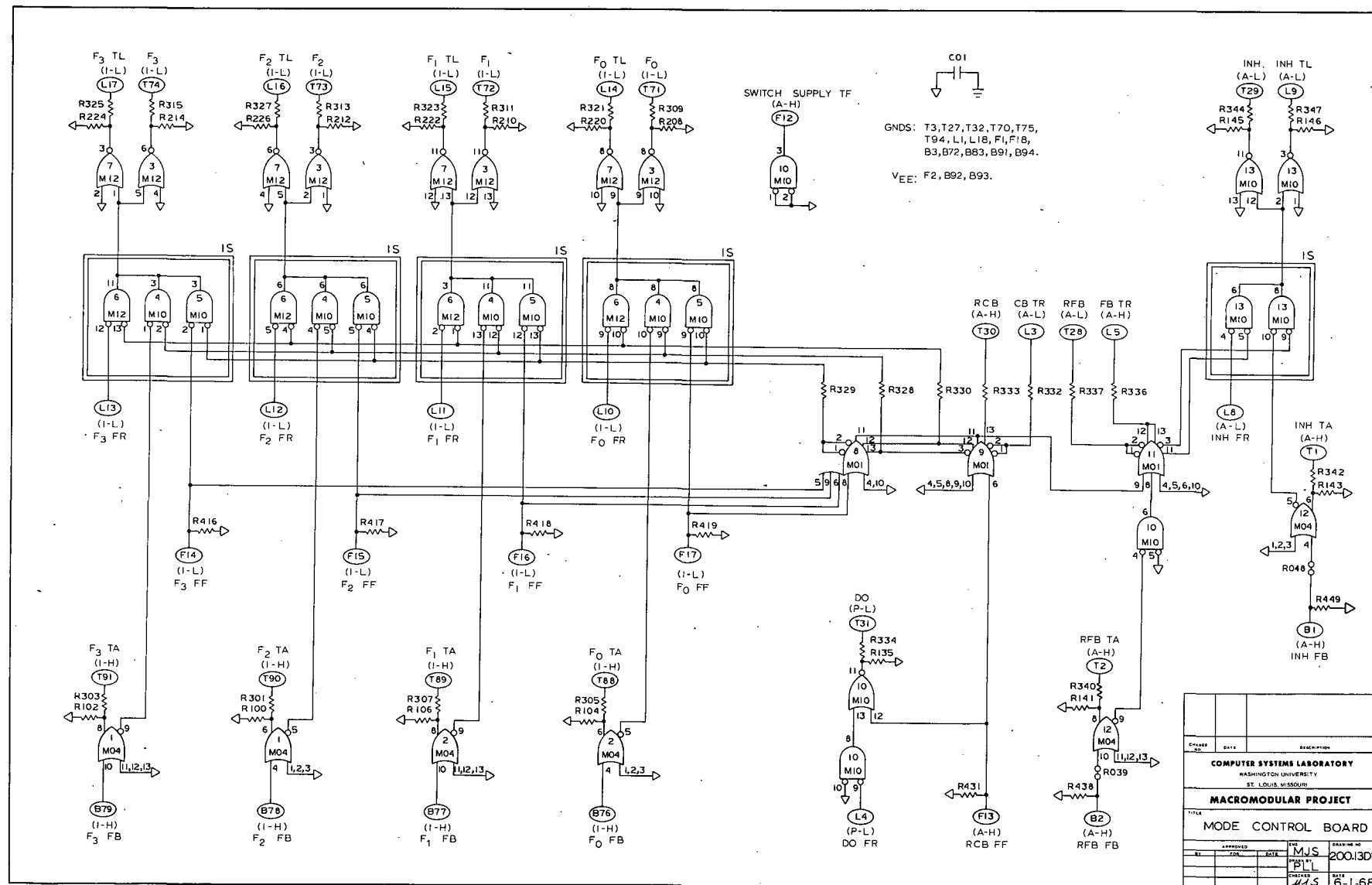
The function of this hole is to take the signal from one surface of the circuit board to the other surface. This type of information has been deleted on the revised drawings discussed in section 3.

B) The numbers 1 and 2 that occur at the ends of resistors, capacitors, and diodes are engineering aids that were useful at a specific phase of the circuit board design process. These numbers should be ignored.

C) The character string that identifies a signal entering (or leaving) a circuit board can be considered a single tag. Somewhere within this tag there is either an isolated L or H, or there is a -L or a -H. These are the polarity indicators. The significance of the indicator depends on the nature of the signal, i.e., depends on whether the signal is a data bit, a condition, or a transition signal. For modules other than the Multiply and Interlock modules, an asterisk identifies the signal as a transition signal and the polarity indicator thus indicates the preset polarity for the signal. Except for this, the nature of the signal is not indicated in the tag.

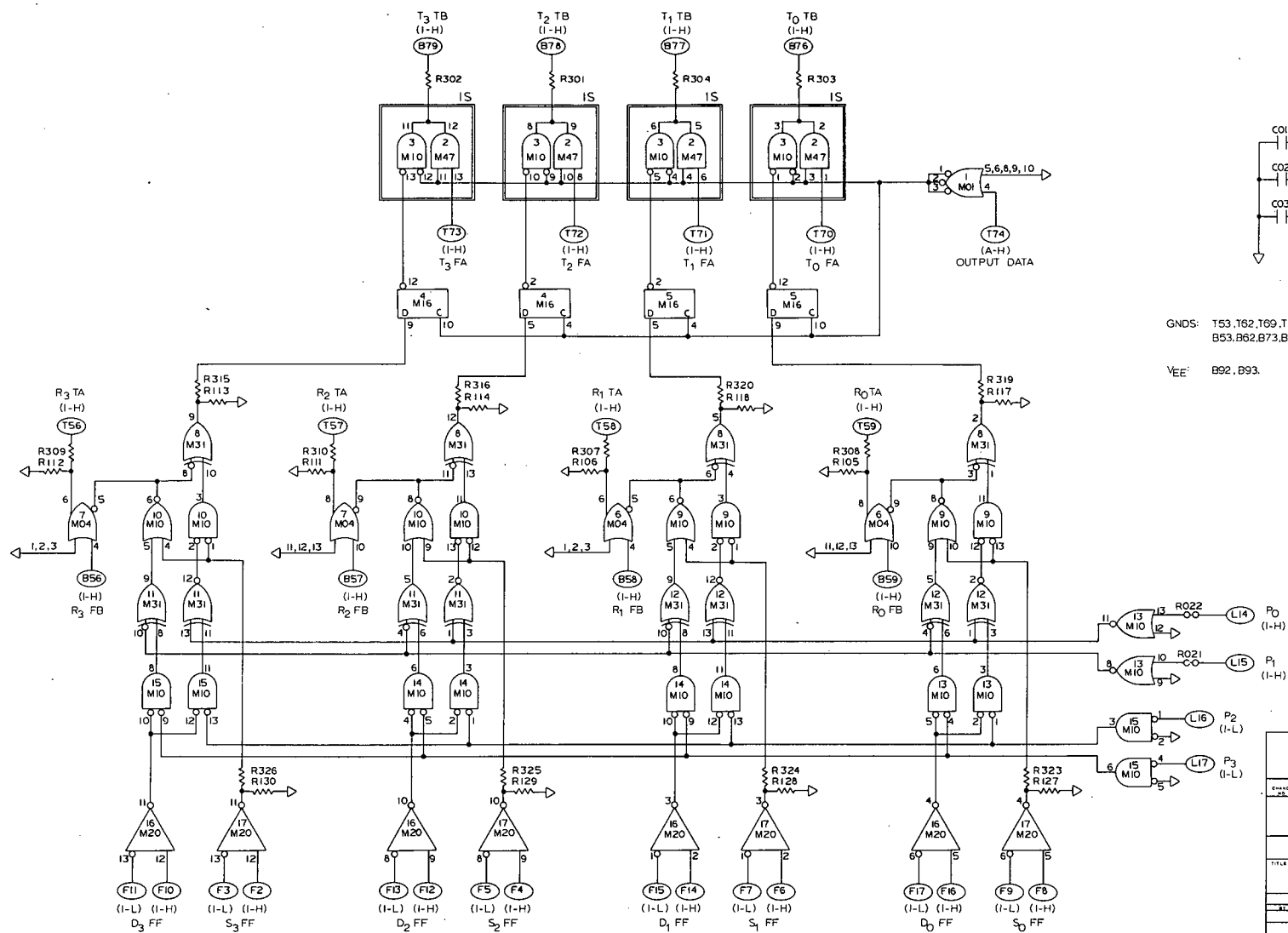


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APPROVED			ENG
BY	FOR	DATE	<i>TJC</i>
			DRAWN BY
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			CHECKED
			<i>T.P.C.</i>
			DRAWING NO
			200.5D3
			DATE
			10-31-68



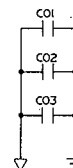
V_{FE} : B92, B93.

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BY	FILE	DATE	MJS 8/11/68	201.20
			APPROVED DATE 8-1-68	6-1-68

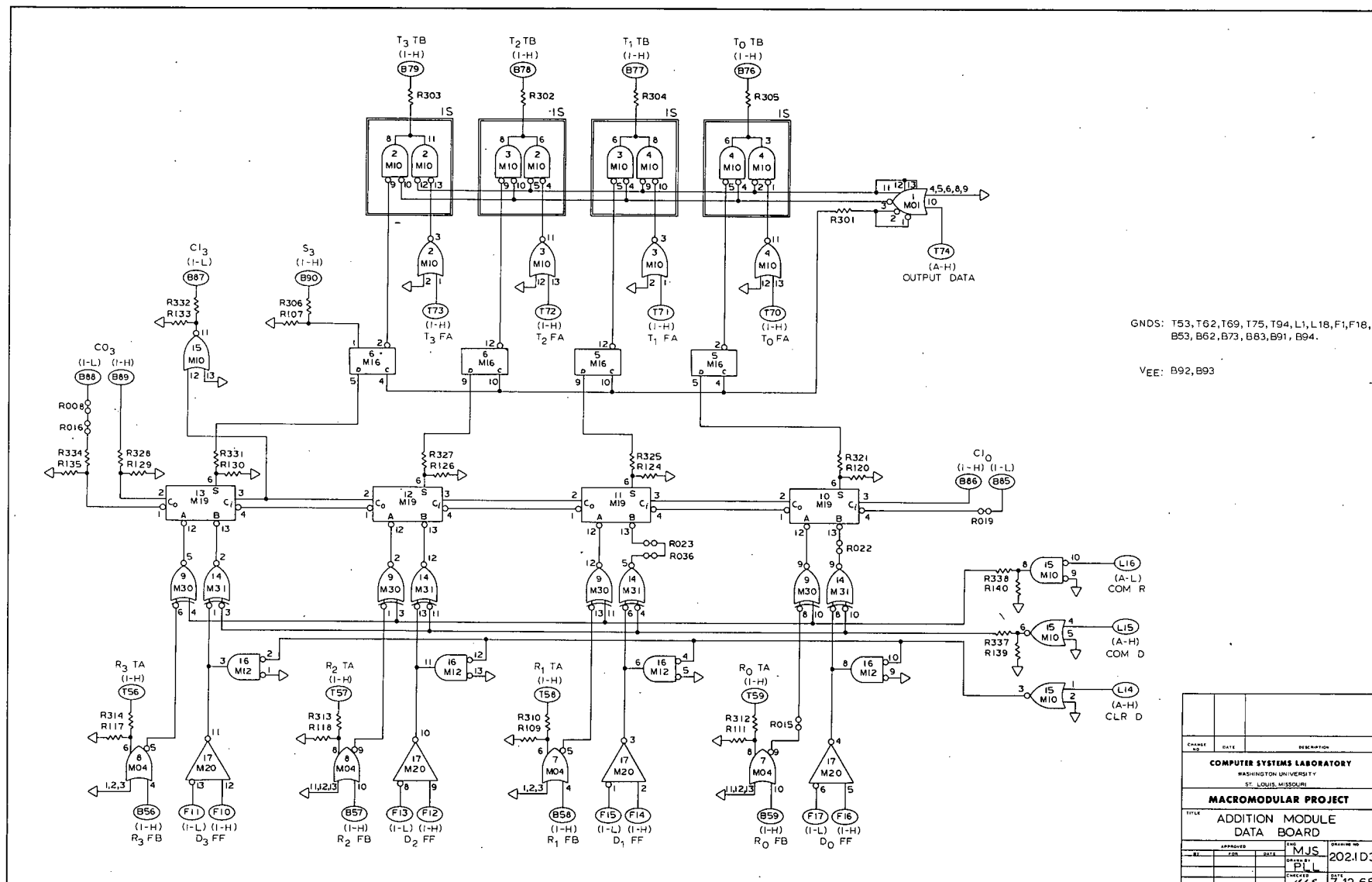


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VEE: B92, B93.



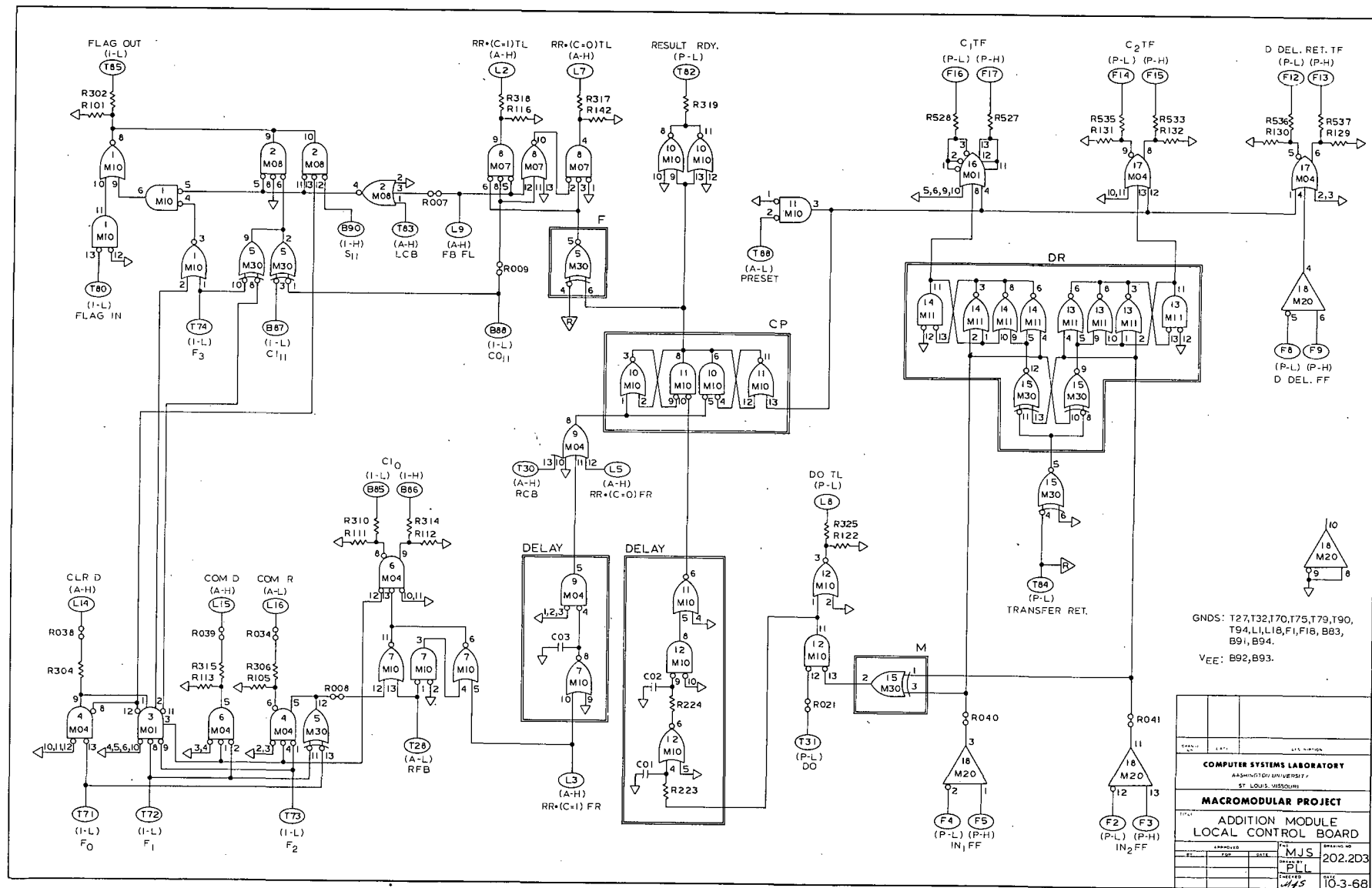
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ST. LOUIS, MISSOURI		
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TITLE		
LOGIC MODULE DATA BOARD		
APPROVED	DATE	BY
DESIGNED	DATE	BY
201.903		11-3-69



GNDS: T53,T62,T69, T75, T94, L1,L18,F1,F18,
B53, B62,B73, B83,B91, B94.

V_{FF}: B92, B93

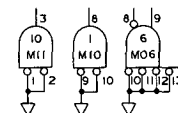
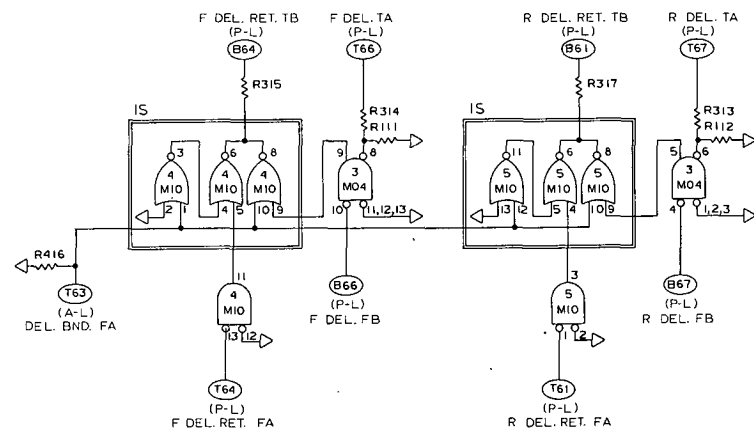
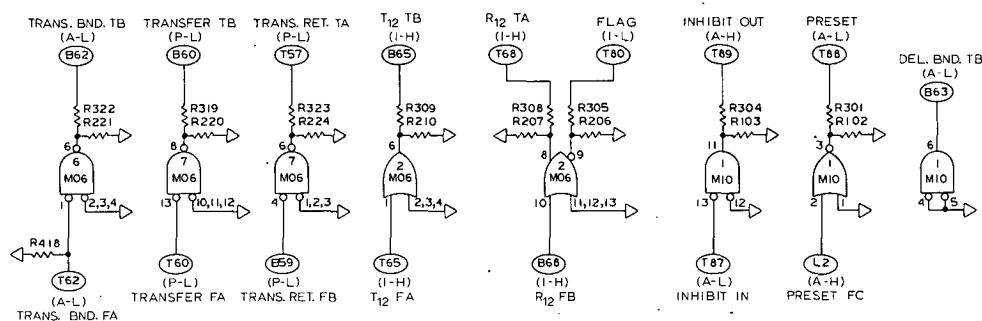
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BY	FOR	DATE	MJS	2021.D	
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			WLS	7-12-68	



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ST. LOUIS, MISSOURI			
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APPROVED	DATE	DATE	DATE
MJS	202.203		
PL			
DATE	DATE	DATE	DATE
10-3-68			

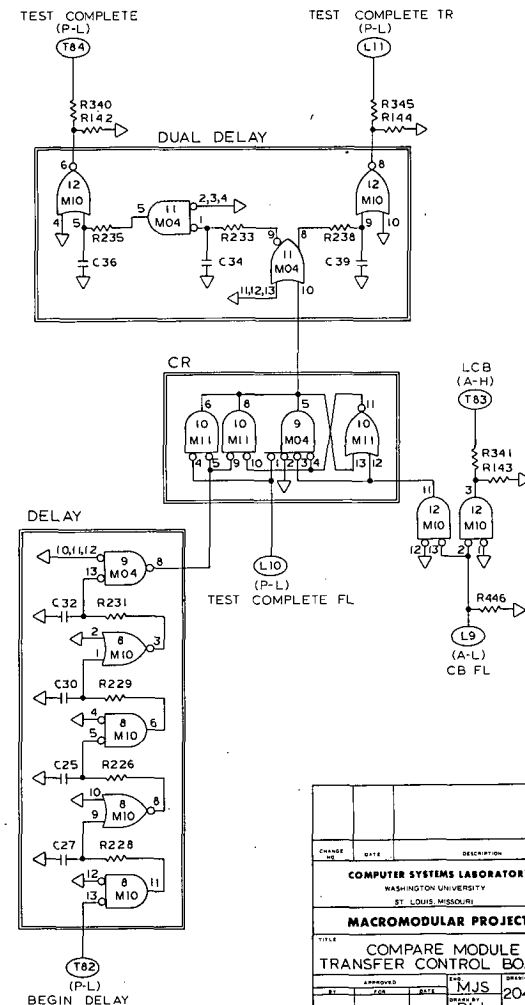
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BY	FOR	DATE	203.1.D
			DRAWN BY P.T.L. CHECKED BY 7.17.68

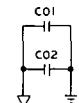
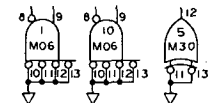
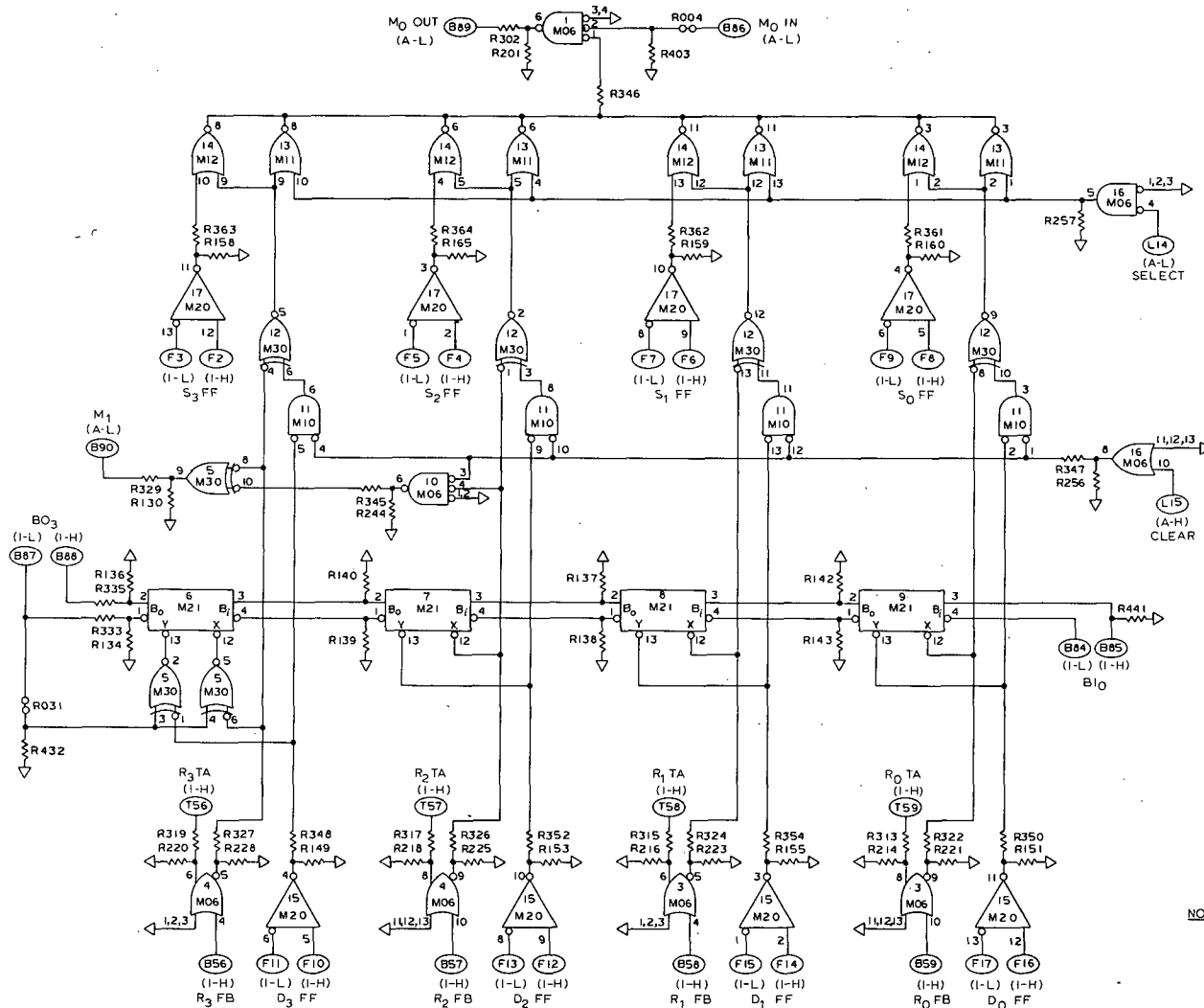


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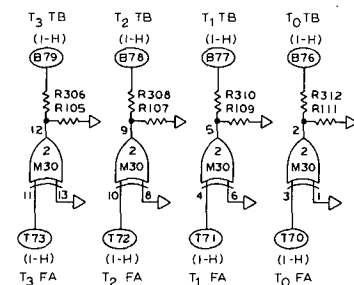
VEE: B92, B93.



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WASHINGTON UNIVERSITY		
ST. LOUIS, MISSOURI		
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TITLE COMPARE MODULE		
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APPROVED	DATE	DESIGNED BY
BY	DATE	BY
CHECKED	DATE	BY
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		10-31-68

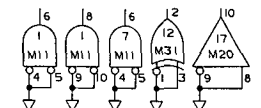
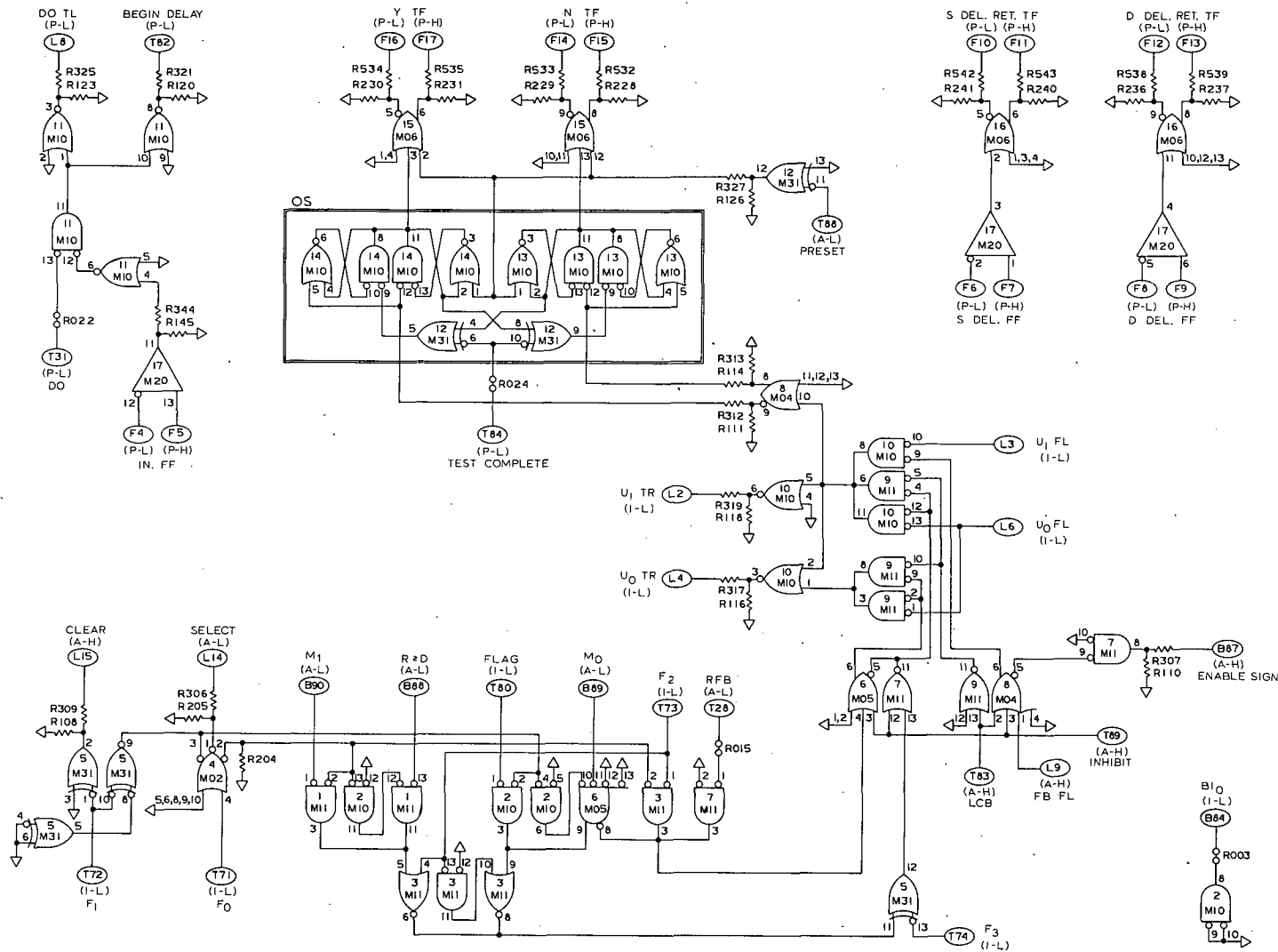


GNDS: T53, T62, T69, T75, T94,
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B62, B73, B83, B91, B94.
V_{EE}: B92, B93.



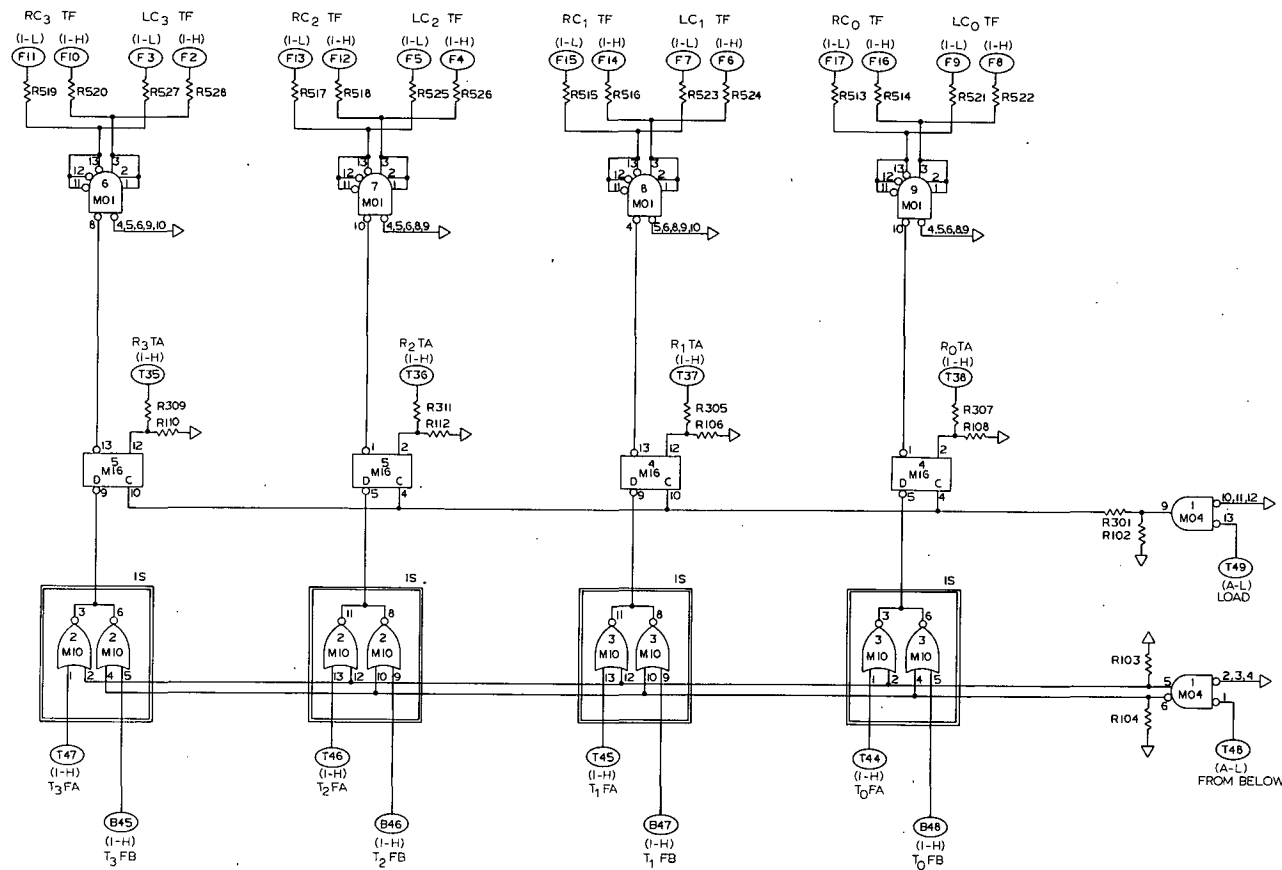
NOTE
MOD 1: OMIT R031
MOD 3: OMIT R333

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		MJS 2044D3
APPROVED	DATE	DESIGNER
		BT
CHECKED	DATE	DESIGNER
		7-29-68



GNDS: T27, T32, T70, T75, T79, T90,
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B91, B94.
V_{EE}: B92, B93.

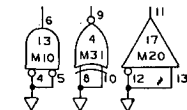
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2		204.1003
3		10-31-68



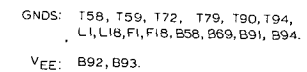
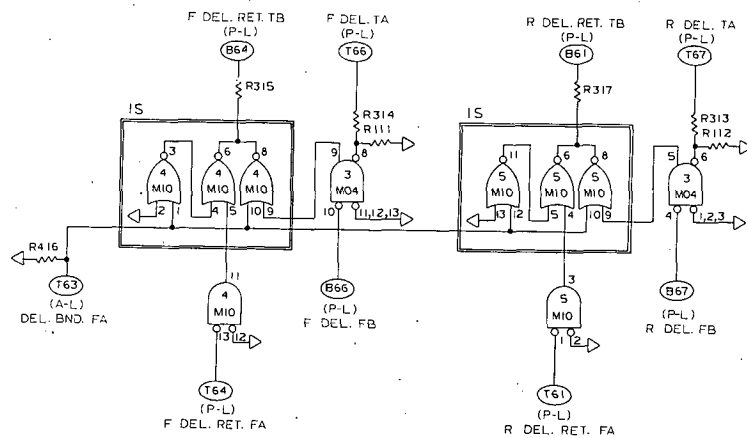
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F1, F18, B44, B49, B91, B94

VEE: B92, B93

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WASHINGTON UNIVERSITY		
ST. LOUIS, MISSOURI		
MACROMODULAR PROJECT		
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APPROVED	DATE	BY
MJS	205.1D3	
PL		
CHECKED	DATE	BY
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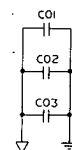
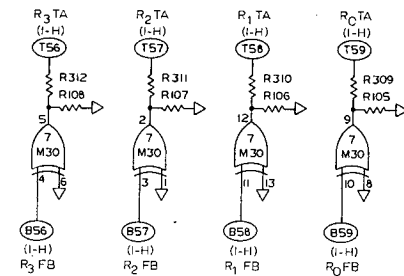
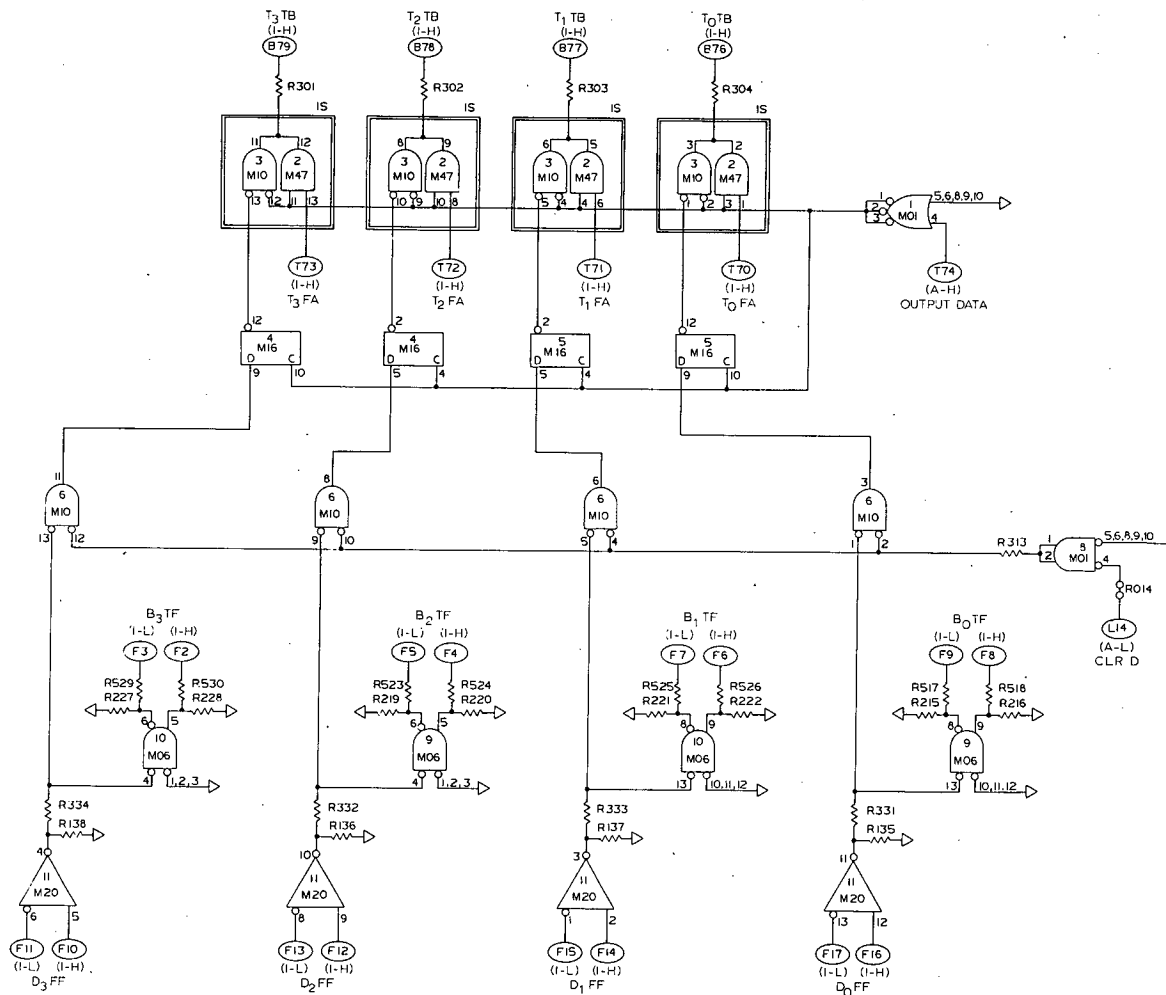


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TITLE		
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APPROVED		SERIAL
BY	FOR	DATE
		MJS
		205.203
		PFL
		CHECKED
		9-3-68



NAME		DATE		PAGE NO.	
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<p align="center">MACROMODULAR PROJECT</p>					
<p align="center">1st SEM</p>					
<p align="center">DECODE MODULE TRANSFER CONTROL BOARD</p>					
PROGRAM		DATE		PAGE NO.	
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		MJS			
		PIL			
		JES			
		DATE		10:31-6B	

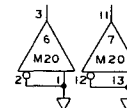
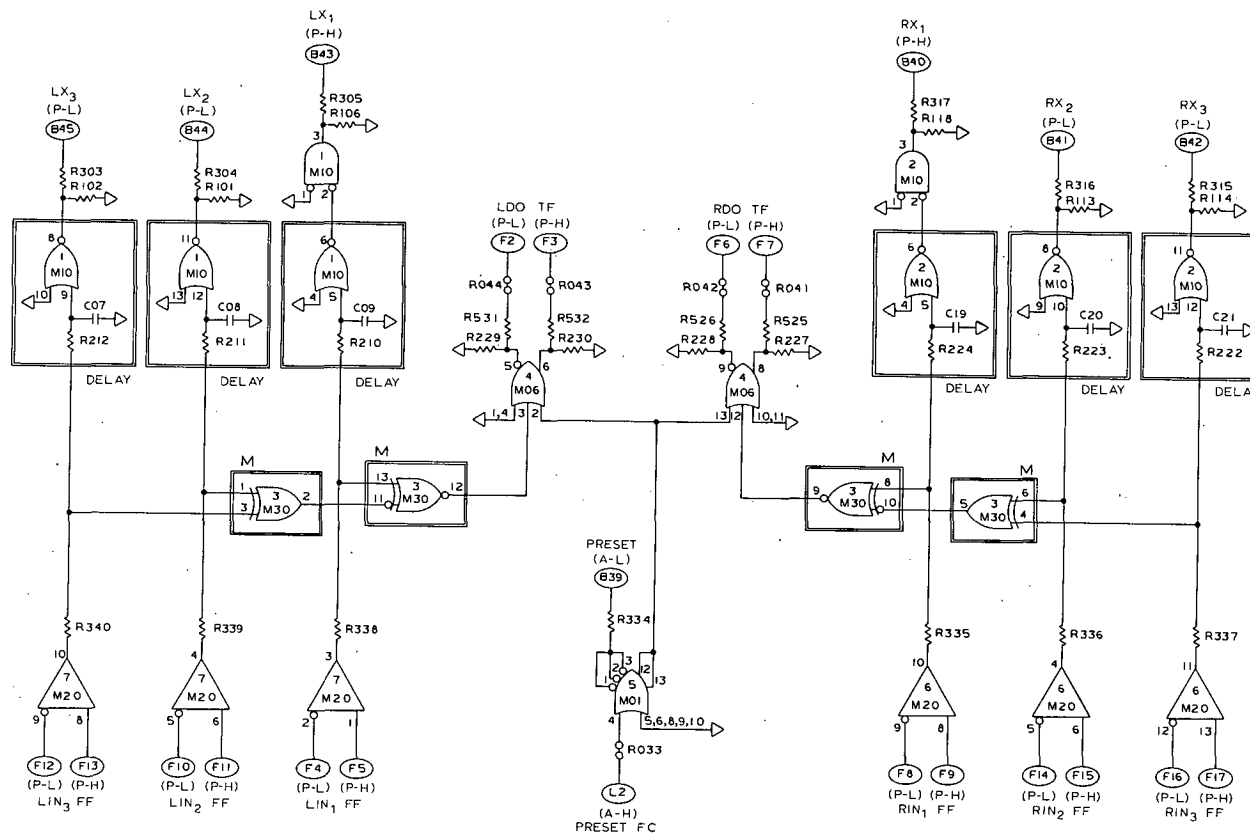




GNDS: T53, T62, T69, T75, T79, T94, L1, L18,
F1, F19, B53, B62, B73, B83, B91, B94

VEE: B92, B93

DATE	REV	DESCRIPTION
207.8D3	1	207.8D3
COMPUTER SYSTEMS LABORATORY		
WASHINGTON UNIVERSITY		
ST. LOUIS, MISSOURI		
MACROMODULAR PROJECT		
LOAD MODULE		
DATA BOARD		
APPROVED	DATE	BY
MJS	207.8D3	207.8D3
CHECKED	DATE	BY
207.8D3	3-2-70	207.8D3

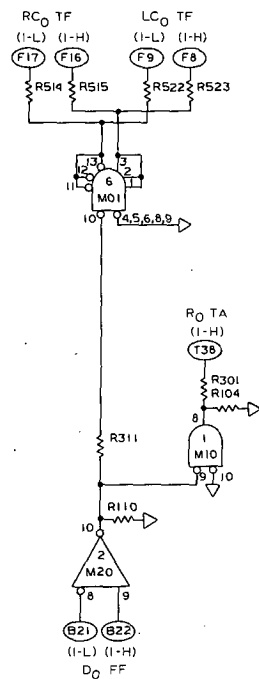
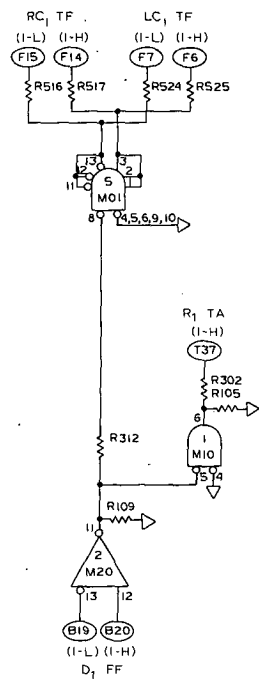
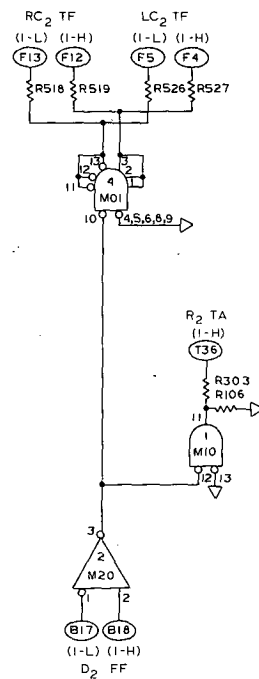
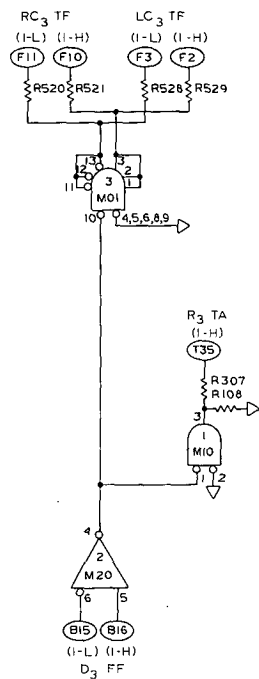


GNDS: T94, L1, L18, F1, F18,
B34, B46, B91, B94.
VEE: B92, B93.

NOTE

PREFIX R: RIGHT CALL UNIT.
PREFIX L: LEFT CALL UNIT.

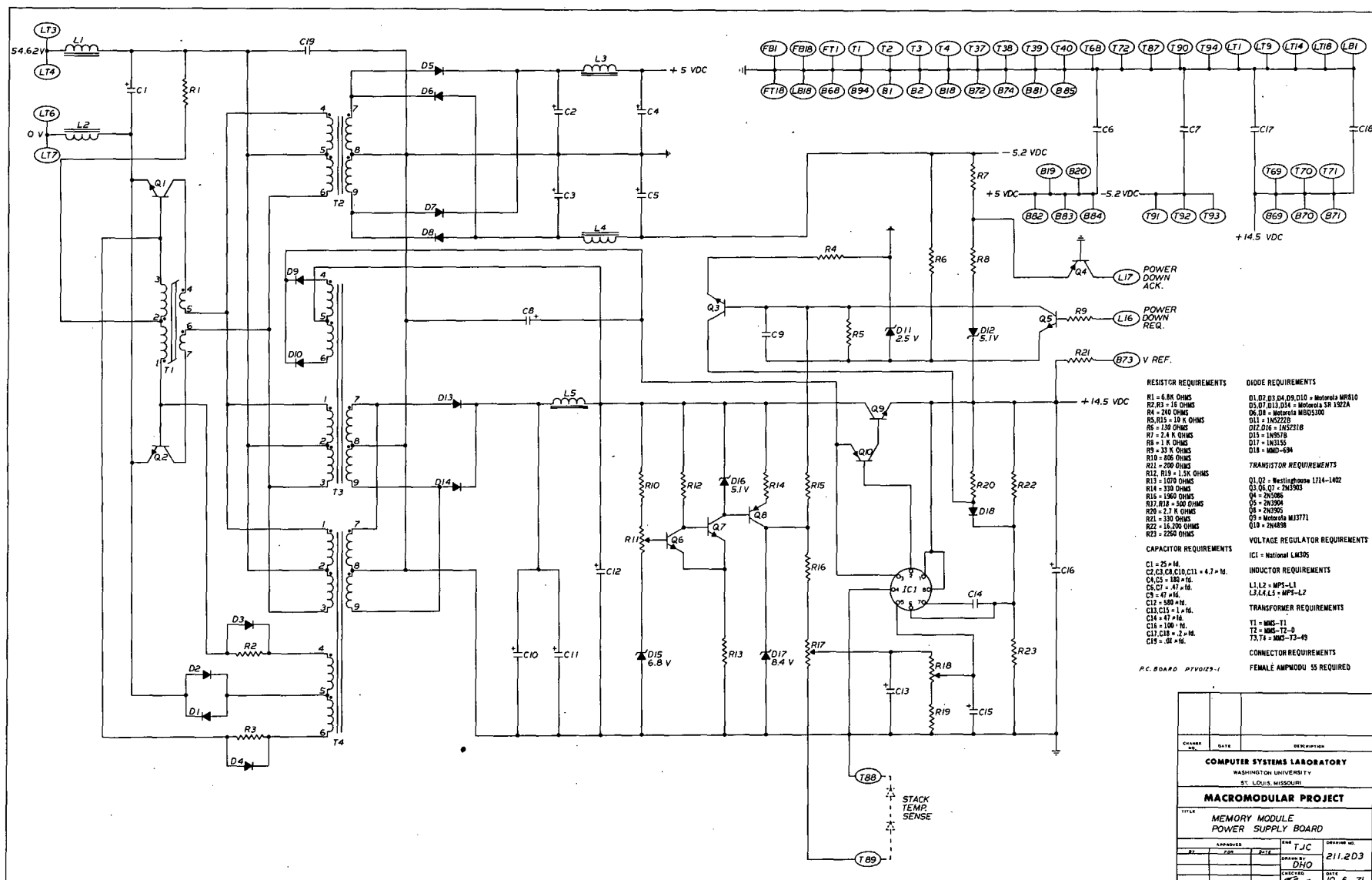
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ST. LOUIS, MISSOURI		
MACROMODULAR PROJECT		
TITLE		
CALL MODULE MERGE BOARD		
DESIGNED BY	DATE	DRAWING NO.
MJS	208.203	
BY	DATE	BY
PL	3-24-69	



GNDS: T32, T41, T94, L1, L18, F1, F18, B14, B23, B91, B94.
V_{EE}: B92, B93.

CHANGE NO.	DATE	DESCRIPTION
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APPROVED	DATE	DESIGNED BY
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		210.1D3
		7-19-68

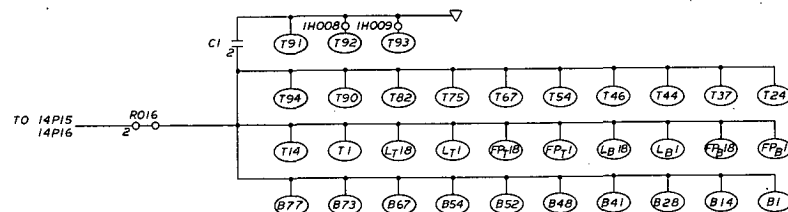
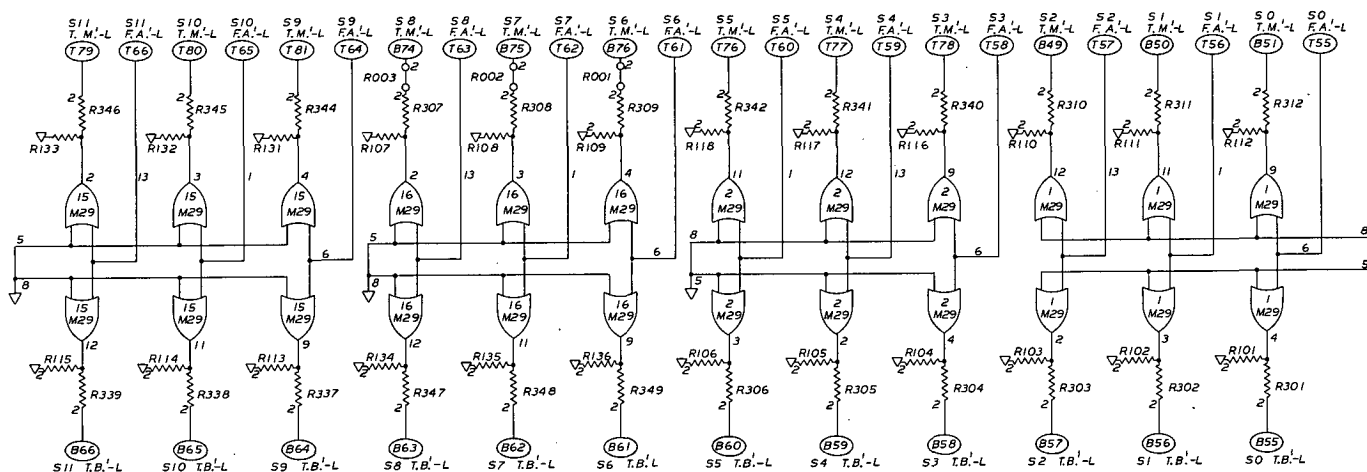
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**EMPLOYEE		END	DRAWING NO.
BY	FOR	MJS	210.2D3
-	-	FILE	
-	-	CHECKED	
-	-	DATE	7-19-68



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3	10-6-71	ST. LOUIS, MISSOURI
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5	10-6-71	TITLE: MEMORY MODULE
6	10-6-71	POWER SUPPLY BOARD
7	10-6-71	DESIGNED BY: TJC
8	10-6-71	DESIGNED BY: DHO
9	10-6-71	DESIGNED BY: DHO
10	10-6-71	DESIGNED BY: DHO
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99	10-6-71	DESIGNED BY: DHO
100	10-6-71	DESIGNED BY: DHO

GROUND, POWER CONNECTIONS AND
PARTS LIST INCLUDED IN LISTING
ON DWG. NO. 211.304
(MEMORY ADDRESS BUFFER)

CHANGE NO.	DATE	DESCRIPTION
		COMPUTER SYSTEMS LABORATORY
		WASHINGTON UNIVERSITY
		ST. LOUIS, MISSOURI
		MACROMODULAR PROJECT
TITLE		B1 DIRECTIONAL DATA BUSS
		MEMORY MACROMODULE
APPROVED	DATE	DESIGNED BY
BY	FOR	DATE
		211.303
		9-30-71



INTEGRATED CIRCUIT IDENTIFICATION

1. M29	11. M47B	21. M06C
2. M29	12. M47B	22. M06C
3. M47B	13. M47B	23. M06C
4. M47B	14. M47B	24. M06C
5. M47B	15. M29	25. M06C
6. M47B	16. M29	26. M06C
7. M47B	17. M06C	27. M06C
8. M47B	18. M06C	28. M06C
9. M47B	19. M06C	29. M06C
10. M47B	20. M06C	

INTEGRATED CIRCUIT REQUIREMENTS

M06B	1
M06C	12
M29	4
M47B	12

RESISTOR REQUIREMENTS

R0XX = ZERO OHMS	17 REQUIRED
R1XX = 1,500 OHMS	48 REQUIRED
R2XX = 750 OHMS	12 REQUIRED
R3XX = 121 OHMS	49 REQUIRED

CONNECTOR REQUIREMENTS

AMP MODU FEMALE	11A REQUIRED
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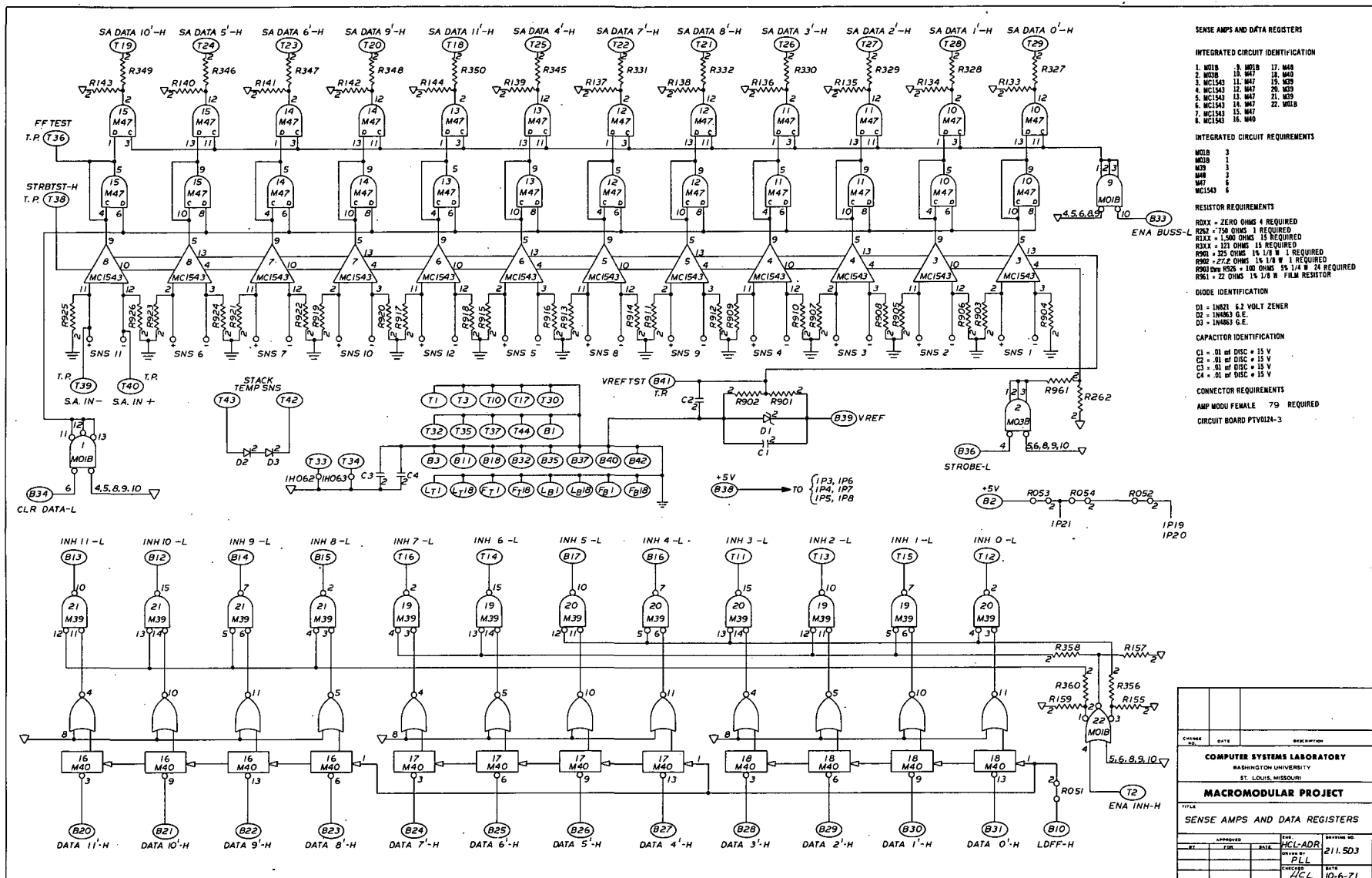
CAPACITOR IDENTIFICATION

C01 = .01 uF DISC	15V
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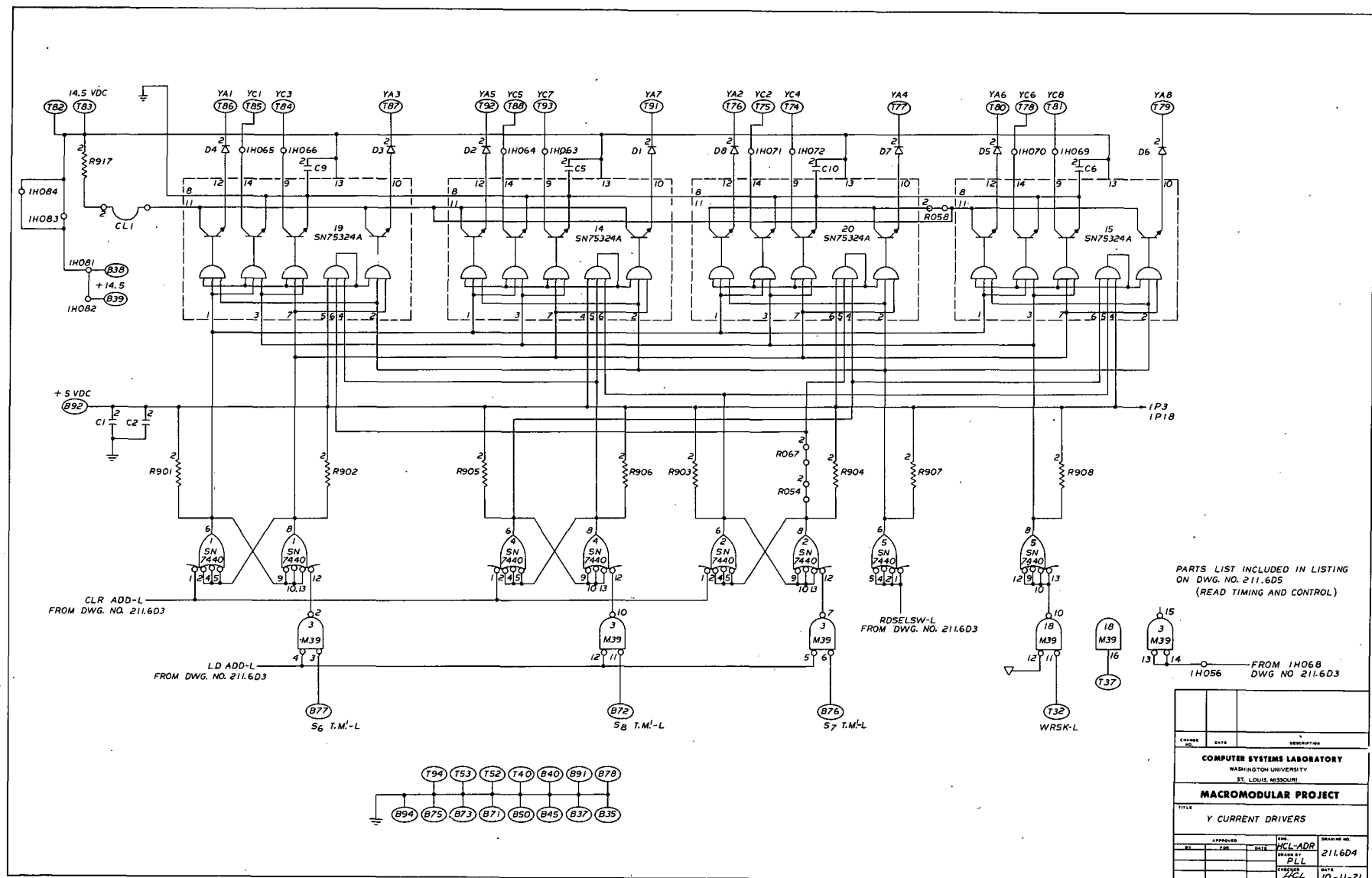
PC BOARD PTV0109-2

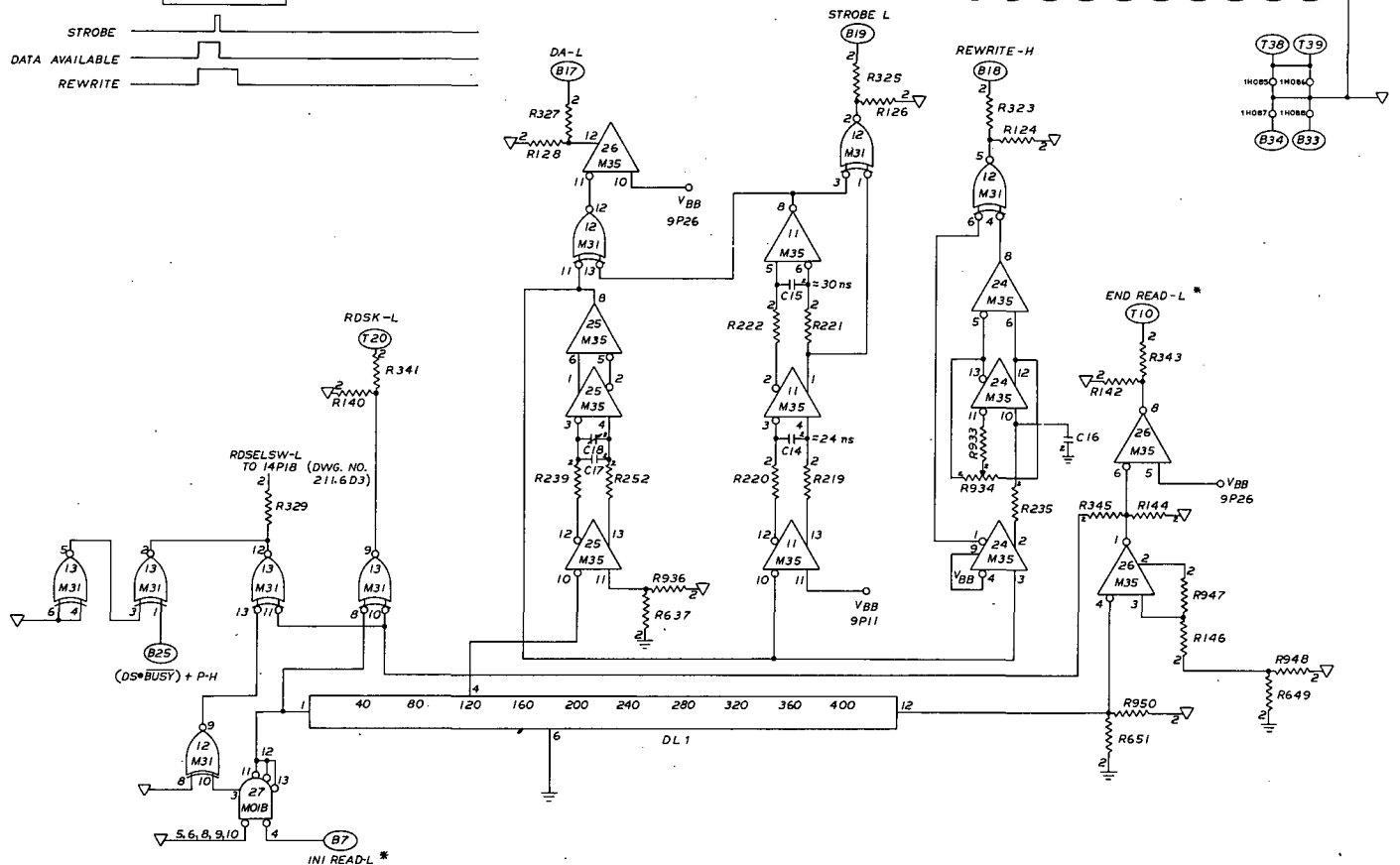
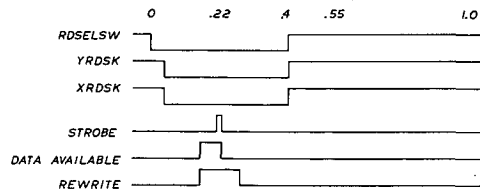
LOGIC FOUND ON DWG NO 211.3D3
(BI DIRECTIONAL DATA BOARD)

CHANGED BY	DATE	DESCRIPTION
COMPUTER SYSTEMS LABORATORY WASHINGTON UNIVERSITY ST. LOUIS, MISSOURI		
MACROMODULAR PROJECT		
TITLE MEMORY ADDRESS BUFFER		
APPROVED BY	DATE	REVISION NO.
BY	DATE	211.3D4
BY	DATE	PL L
BY	DATE	77C L
BY	DATE	10-1-71



CHANGE NO.	DATE	REVISION	
<p align="center">COMPUTER SYSTEMS LABORATORY WASHINGTON UNIVERSITY ST. LOUIS, MISSOURI</p>			
MACROMODULAR PROJECT			
TITLE			
SENSE AMPS AND DATA REGISTERS			
APPROVED		DRAWN BY	DATE
BT	FOR	FILED-ADR	211.503
		REVIEWED	
		PLD	
		CHECKED	
		DATE	10-6-71





PARTS LIST FOR DRAWINGS 211.601, 211.604, 211.605

INTEGRATED CIRCUIT IDENTIFICATION

1. SN7440	10. SN7440	19. SN75324A
2. SN7440	11. M35	20. SN75324A
3. M35	12. M31	21. SN75324A
4. SN7440	13. M31	22. SN75324A
5. SN7440	14. SN75324A	23. M31B
6. SN7440	15. SN75324A	24. M35
7. SN7440	16. SN75324A	25. M35
8. M35	17. SN75324A	26. M35
9. SN7440	18. M35	27. M31B

INTEGRATED CIRCUIT REQUIREMENTS

M31B 2 EA.
M31 7 EA.
M35 4 EA.
M35 3 EA.
SN7440 8 EA.
SN75324A 8 EA.

RESISTOR REQUIREMENTS

R1XX = 1500 OHMS 7 EA.
R2XX = 150 OHMS 1 EA.
R3XX = 121 OHMS 3 EA.
R4XX = 130 OHMS 3 EA.
R500 100K 1/4W 1% 1 EA.
R511, R518 = 29.2 OHMS 3W
R536, R546, R550 = 430 OHMS
R553 = 390 OHMS
R547 = 2.000 OHMS
R534 = 2.000 OHM TRIMPOT

DIODE REQUIREMENTS

D1 thru D16 = MMD-694 (CSL DIODE)

CONNECTOR REQUIREMENTS

AMP MODU FEMALE NO. 8563-4 94 EA.

PRINTED CIRCUIT BOARD

PTV604-4

CAPACITOR REQUIREMENTS

C1 thru C4, C19 = .01 and .05 V 5 EA.
C5 thru C12 = .01 and .05V
C13 = 4.7 μ F ELECTROLYTIC
C15 = 30 μ F
C16 = 100 μ F
C18 = 45-50 μ F VARIABLE
C14 = 27 pF
C17 (CM17)

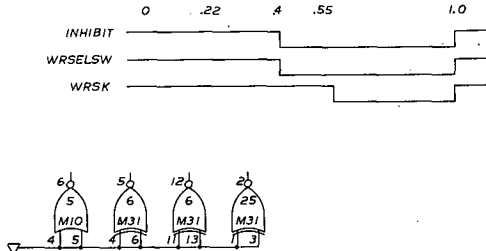
CURRENT LOOPS

CL1, CL2, NO.22 STRANDED WIRE 2 IN. LONG
TEFLON INSULATED

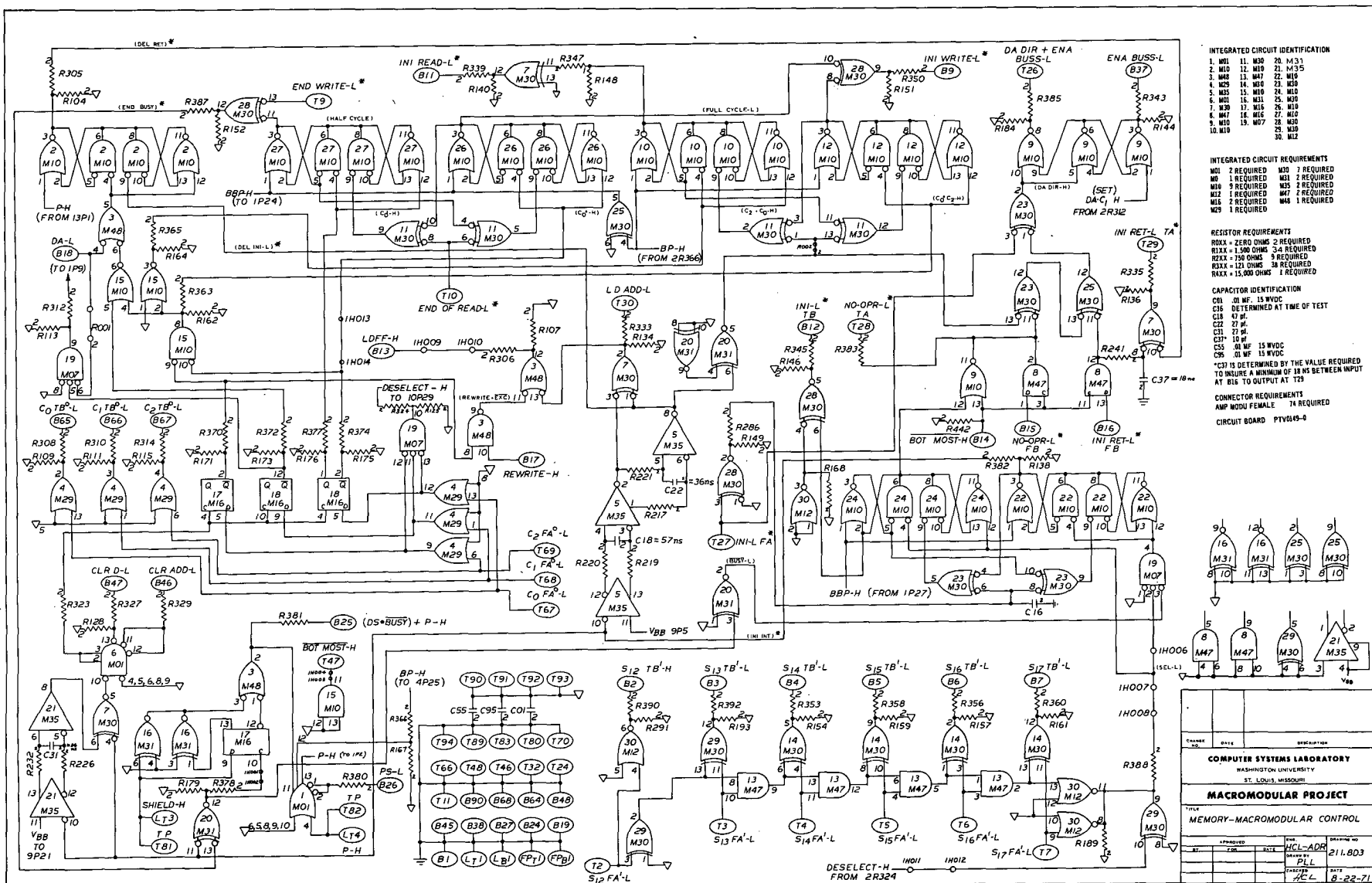
DELAY LINE

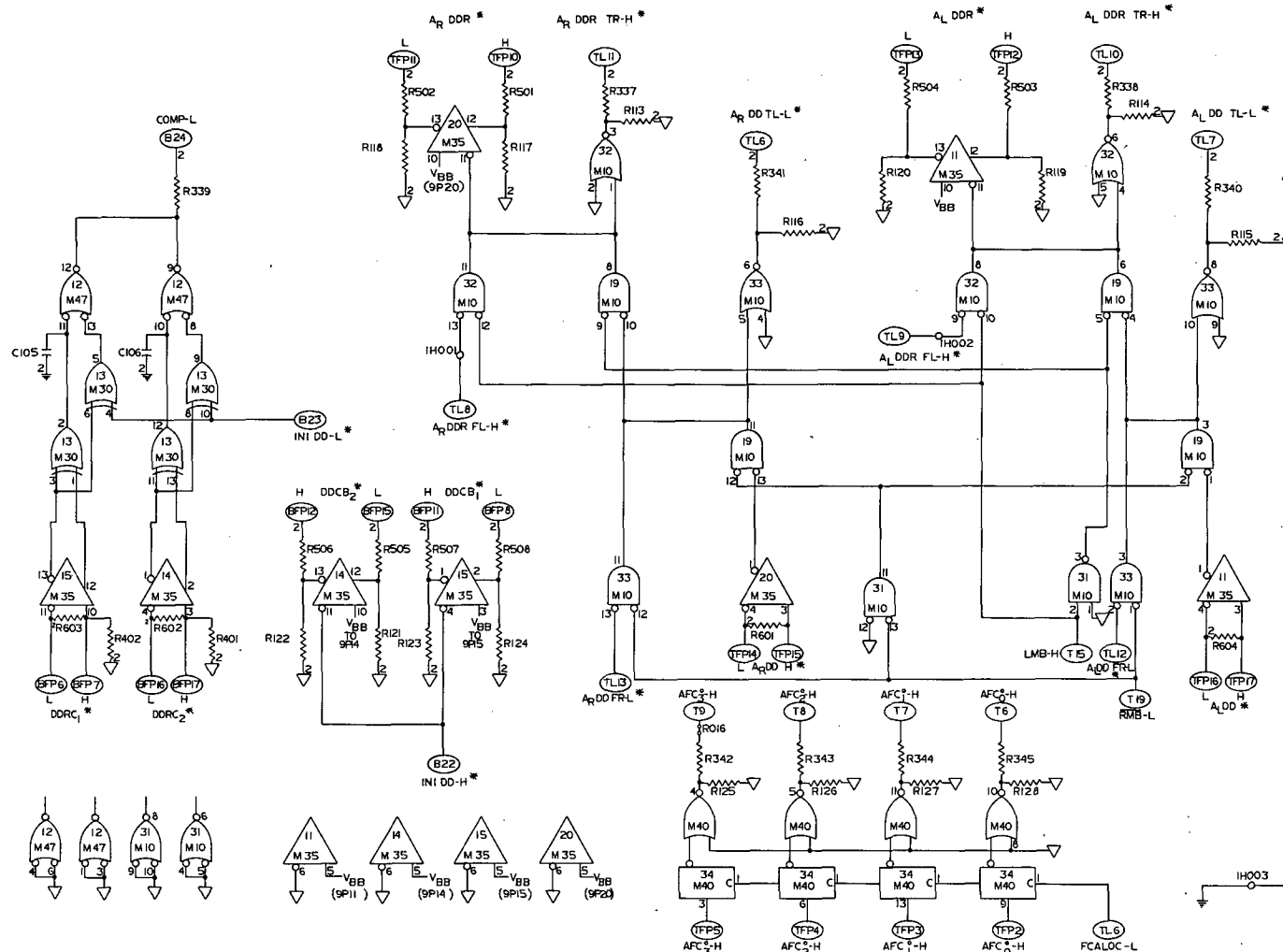
DL1 = PE-7118

CHANGES	DATE	DESCRIPTION
<p>COMPUTER SYSTEMS LABORATORY WASHINGTON UNIVERSITY ST. LOUIS, MISSOURI</p>		
<p>MACROMODULAR PROJECT</p>		
<p>TITLE READ TIMING AND CONTROL</p>		
APPROVED	DATE	DRAWING NO.
BY	DATE	211.605
CHECKED	DATE	3-21-72



CHARGE NO.	DATE	DESCRIPTION
<p align="center">COMPUTER SYSTEMS LABORATORY WASHINGTON UNIVERSITY ST. LOUIS, MISSOURI</p> <p align="center">MACROMODULAR PROJECT</p>		
TITLE		
WRITE TIMING AND CONTROL		
APPROVED		FILE
BY	DATE	FILE NO.
		217.705
		PLI
		PLCL
		DATE
		5-3-72





Parts List for Drawings 212.3D3 and 212.3D4
Integrated Circuit Identification

1. M35	12. M47	23. P85A10
2. P8582	13. P858	24. P85A10
3. P85A10	14. P85	25. P85A10
4. P85A10	15. M35	26. P85A10
5. P85A10	16. P8582	27. P85A10
6. P85A10	17. P8582	28. P85A10
7. P85A10	18. M35	29. P8582
8. P85A10	19. M10	30. M35
9. P8582	20. M35	31. M10
10. P8582	21. M35	32. M10
11. M35	22. P8582	33. M10

Integrated Circuit Requirements

M10	4 each
M30	1 each
M35	8 each
M47	1 each
P8582	7 each
P85A10	17 each
M40	1 each

Resistor Identification

R10X = zero ohms	16 required.
R1XX = 1,500 ohms	28 required.
R2XX = 750 ohms	28 required.
R3XX = 101 ohms	45 required.
R4XX = 15,000 ohms	7 required.
R5XX = 120 ohms	4 required.
R601, R604 thru R614 = 470 ohms 12 req.	
R682 = 100 ohms	8 required.
R693 = 500 ohms	8 required.
R694 = 504 ohms	8 required.

Capacitor Identification

C1XX = .01 pfd	4 required
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Connector Requirements

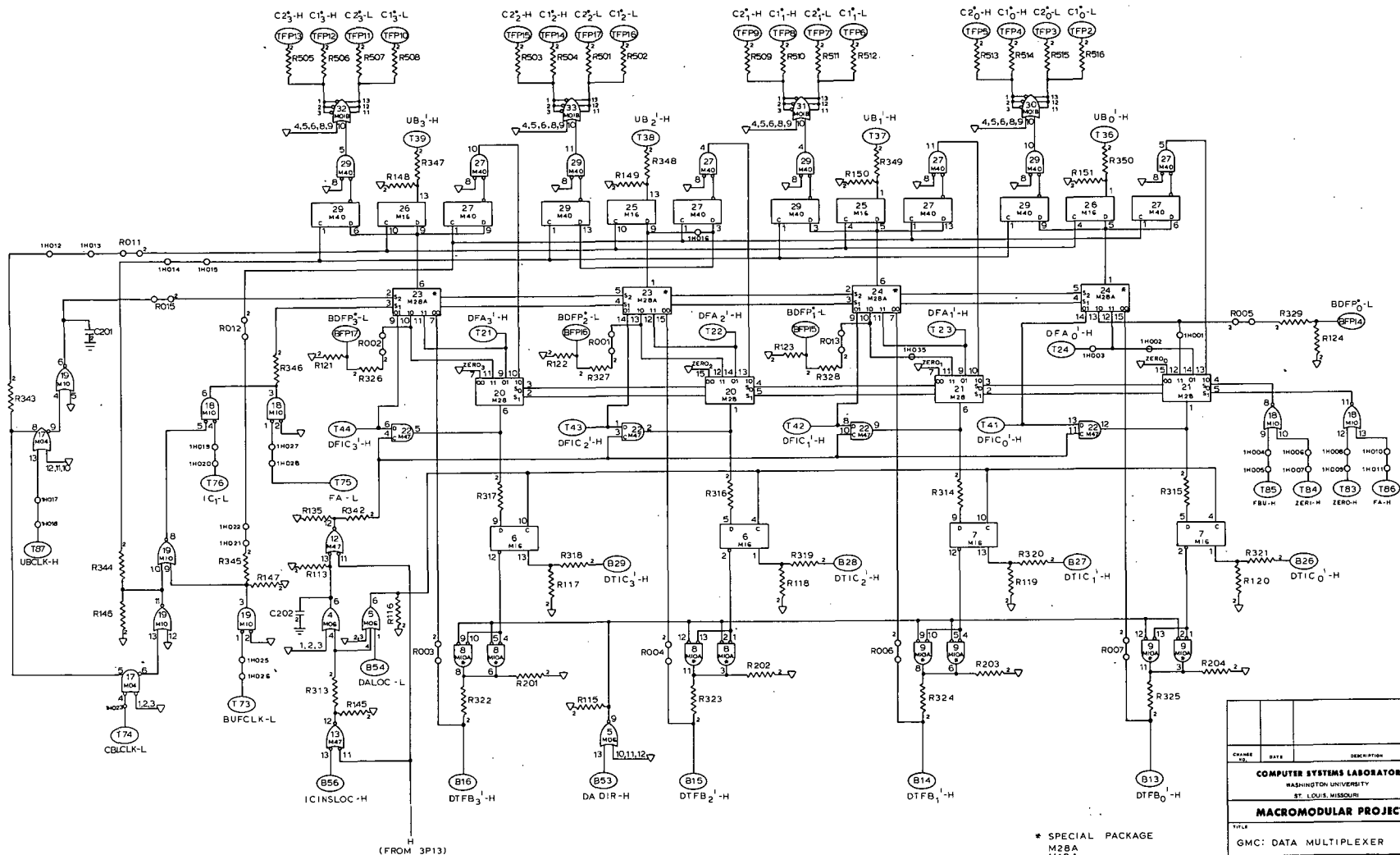
Asp modu Female No. 85863-4	96 req.
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Printed Circuit Board

PTV0156-2

Ground

B50, B54, B57, B58, B60, B62, B65, B67, B71, B72, B73, B74, B75, B76, B77, B78, B79, B80, B81, B82, B83, B84, B85, B86, B87, B88, B89, B90, B91, B92, B93, B94, B95, B96, B97, B98, B99, B100, B101, B102, B103, B104, B105, B106, B107, B108, B109, B110, B111, B112, B113, B114, B115, B116, B117, B118, B119, B120, B121, B122, B123, B124, B125, B126, B127, B128, B129, B130, B131, B132, B133, B134, B135, B136, B137, B138, B139, B140, B141, B142, B143, B144, B145, B146, B147, B148, B149, B150, B151, B152, B153, B154, B155, B156, B157, B158, B159, B160, B161, B162, B163, B164, B165, B166, B167, B168, B169, B170, B171, B172, B173, B174, B175, B176, B177, B178, B179, B180, B181, B182, B183, B184, B185, B186, B187, B188, B189, B190, B191, B192, B193, B194, B195, B196, B197, B198, B199, B200, B201, B202, B203, B204, B205, B206, B207, B208, B209, B210, B211, B212, B213, B214, B215, B216, B217, B218, B219, B220, B221, B222, B223, B224, B225, B226, B227, B228, B229, B230, B231, B232, B233, B234, B235, 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* SPECIAL PACKAGE
M28A
M10A
PARTS LIST INCLUDED IN
LISTING ON DWG. NO. 212.4D4

CHANGE	DATE	DESCRIPTION
1		
COMPUTER SYSTEMS LABORATORY		
WASHINGTON UNIVERSITY		
ST. LOUIS, MISSOURI		
MACROMODULAR PROJECT		
TITLE		
GMC: DATA MULTIPLEXER		
APPROVED	DATE	BY
PL		ADR
DATE		212.4D3
DATE		12-19-72

Integrated Circuit Identification

1. M16	12. M47	23. M28A
2. M16	13. M47	24. M28A
3. M16	14. M28	25. M16
4. M16B	15. M28	26. M16
5. M16	16. M28	27. M40
6. M16	17. M40	28. M20
7. M16	18. M10	29. M40
8. M10A	19. M10	30. M21B
9. M10A	20. M28	31. M21B
10. M20	21. M28	32. M21B
11. M20	22. M47	33. M21B

Integrated Circuit Requirements

M16B	4 ea.	M20	2 ea.
M40	1 ea.	M28	3 ea.
M16	1 ea.	M28A	2 ea.
M10A	2 ea.	M20	1 ea.
M16A	2 ea.	M47	2 ea.
M16	2 ea.	M47	3 ea.

Resistor Requirements

R0XX - zero ohms	75 required
R1XX - 1,500 ohms	50 required
R2XX - 750 ohms	50 required
R3XX - 121 ohms	54 required
R4XX - 15,000 ohms	6 required
R5XX - 20.6 ohms	6 required
R6XX - 130 ohms	6 required

Diode Requirements

D1XX - GE 1N3604	2 required
------------------	------------

Capacitor Requirements

C1XX - .01 ufd	
C2XX - NOT REQUIRED	
C3XX - 62 ufd	

Connector Requirements

Amp Modu Female #65863-4	135 req.
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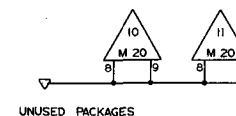
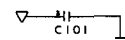
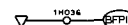
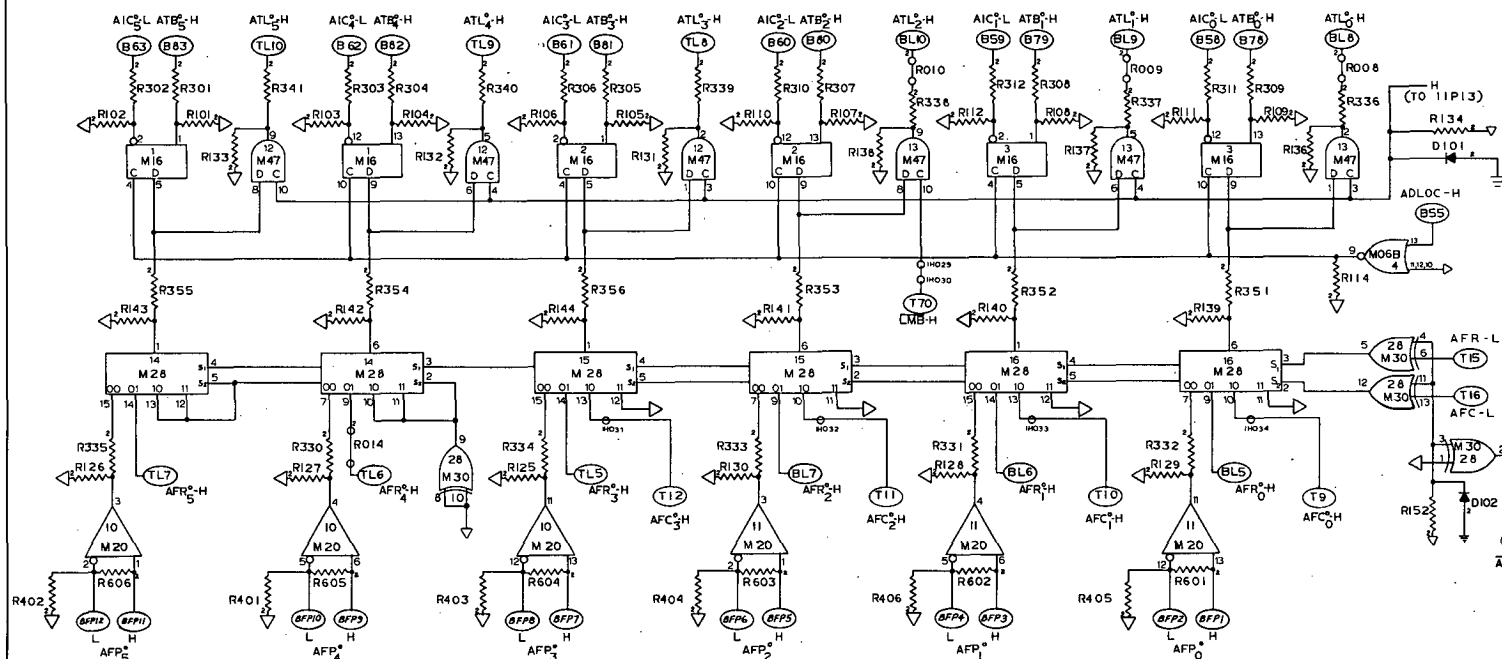
Printed Circuit Board PTV0162-2

Ground: B94, B99, B84, B77, B57, B52, B30, B25, B12, BFP15, B11, B14, B111, T993, T9918, T11, T14, T131, T8, T13, T17, T20, T25, T35, T40, T68, T77, T90, T94

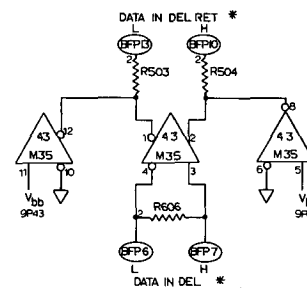
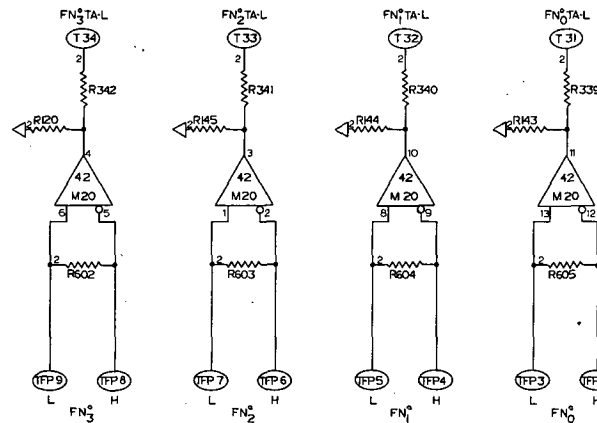
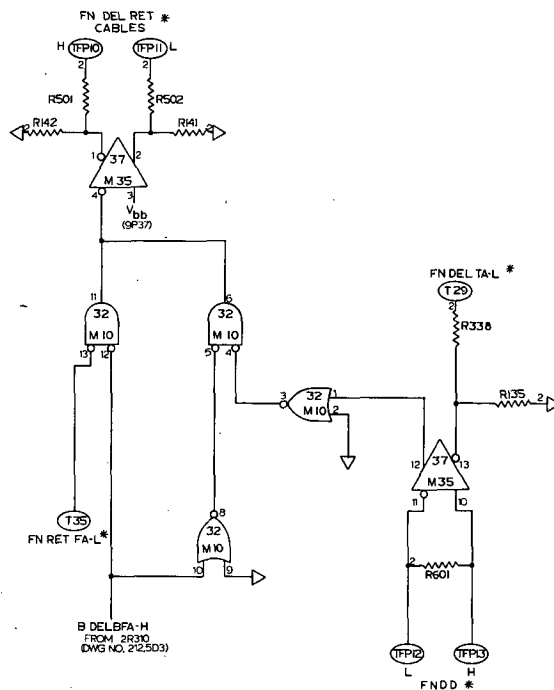
Power: B91, B92, B93, T91, T92, T93

LOGIC FOUND ON 4 BIT DATA BOARD (PTV0162-0)

CHARGE	DATE	DESCRIPTION
COMPUTER SYSTEMS LABORATORY		
WASHINGTON UNIVERSITY		
ST. LOUIS, MISSOURI		
MACROMODULAR PROJECT		
TITLE		
GMC		
ADDRESS MULTIPLEXER		
APPROVED	DATE	BY
CHECKED	DATE	BY



UNUSED PACKAGES

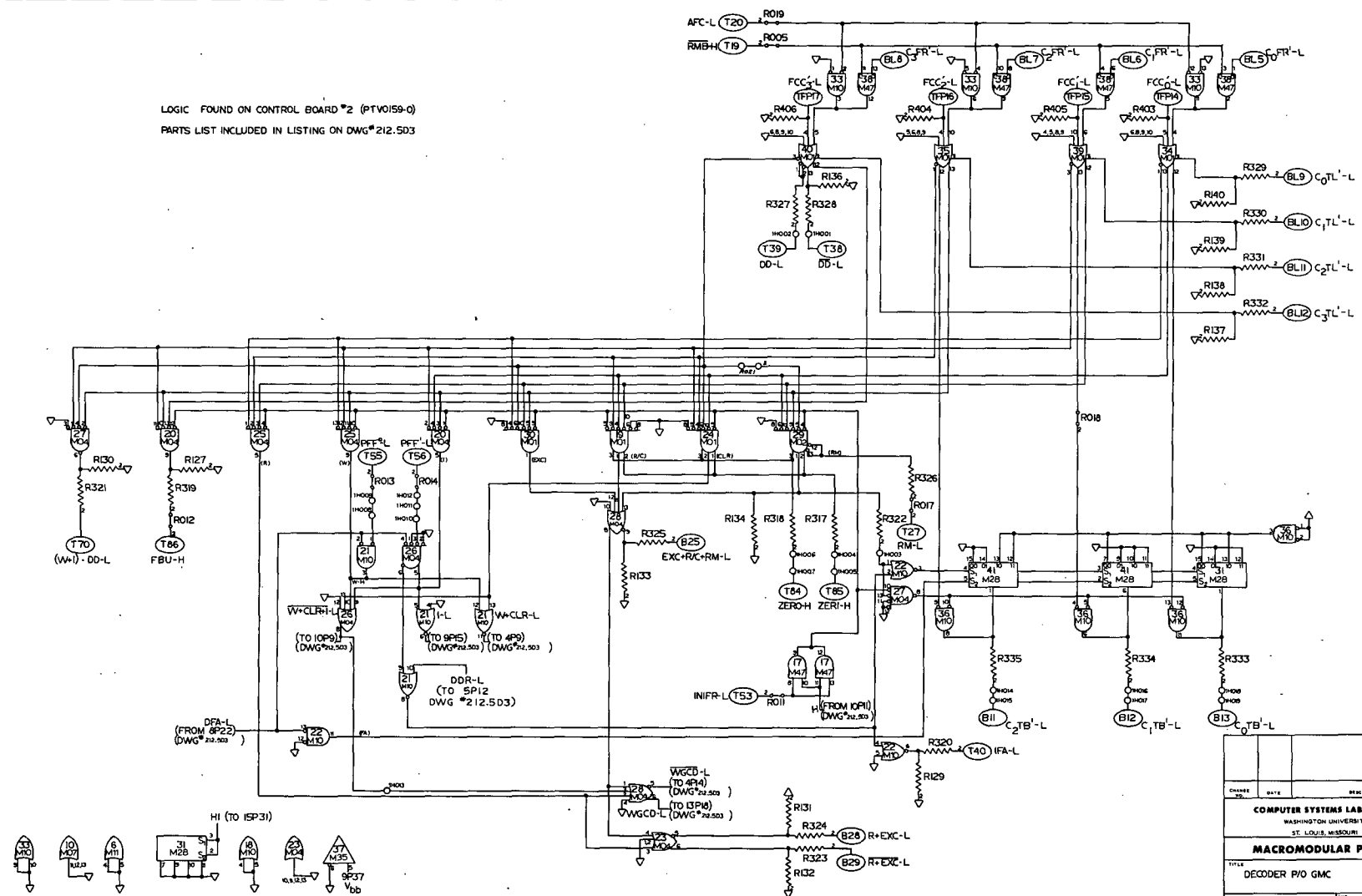


PARTS LIST INCLUDED IN
LISTING ON DWG NO 212.503

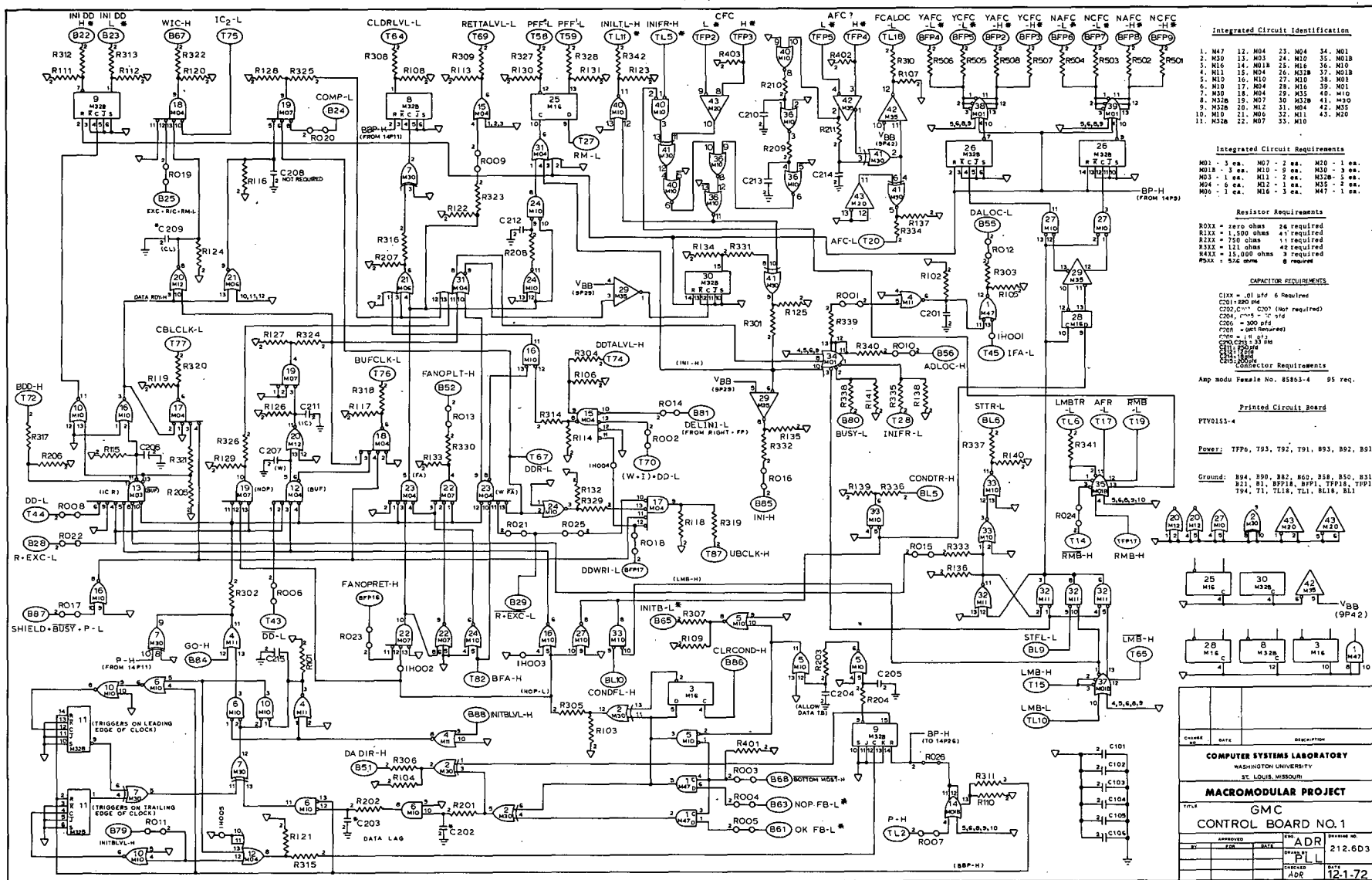
LOGIC FOUND ON CONTROL
BOARD NO. 2 (PTV0159-0)

CHANGES	DATE	DESCRIPTION
1		
COMPUTER SYSTEMS LABORATORY WASHINGTON UNIVERSITY ST. LOUIS, MISSOURI		
MACROMODULAR PROJECT		
TITLE: GMC: MISCELLANEOUS DATA DELIVERY		
APPROVED	DATE	DESIGNED BY
MAC		ADR
CHECKED	DATE	212.504
ADR	12-7-72	

PARTS LIST INCLUDED IN LISTING ON DWG# 212.5D3



CHARGE TO		DATE		DESCRIPTION	
<p align="center">COMPUTER SYSTEMS LABORATORY WASHINGTON UNIVERSITY ST. LOUIS, MISSOURI</p>					
MACROMODULAR PROJECT					
TITLE					
DECODER P/O GMC					
APPROVED			S&B	DRAWING NO.	
BY	FILE	DATE	ADR		
			CHARGED TO MAC	212.505	
			FILE	DATE 1-10-73	



Integrated Circuit Identification

1. M47	12. M04	23. M04	34. M01
2. M30	13. M03	24. M10	35. M01B
3. M16	14. M01B	25. M16	36. M10
4. M11	15. M04	26. M32B	37. M01B
5. M10	16. M10	27. M10	38. M01B
6. M10	17. M04	28. M16	39. M01
7. M30	18. M04	29. M35	40. M10
8. M32B	19. M07	30. M32B	41. M30
9. M32B	20. M12	31. M04	42. M35
10. M10	21. M06	32. M11	43. M20
11. M32B	22. M07	33. M10	

Integrated Circuit Requirements

M01 - 3 ea.	M07 - 2 ea.	M20 - 1 ea
M01B - 3 ea.	M10 - 9 ea.	M30 - 3 ea
M03 - 1 ea.	M11 - 2 ea.	M32B - 5 ea
M04 - 6 ea.	M12 - 1 ea.	M35 - 2 ea
M06 - 1 ea.	M16 - 3 ea.	M47 - 1 ea

Resistor Requirements

R0XX	= zero ohms	26 required
R1XX	= 1,500 ohms	41 required
R2XX	= 750 ohms	11 required
R3XX	= 121 ohms	42 required
R4XX	= 15,000 ohms	3 required

CAPACITOR REQUIREMENTS

```
C:\XX = .01 ufd 6 Required
C201 = 220 pfd
C202, C203 = C207 (Not required)
C204, C205 = 10 pfd
C206 = 300 pfd
C208 = gct Required)
rmp = 1.0 of 3
C200, C203 = 33 pfd
C211 = 250 pfd
C212 = 1 pfd
C213 = 1 pfd
C214 = 1 pfd
C215 = 1 pfd
```

Connector Requirements

App modu Female No. 85863-4 25 rec.

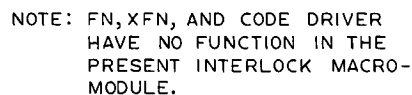
Printed Circuit Board

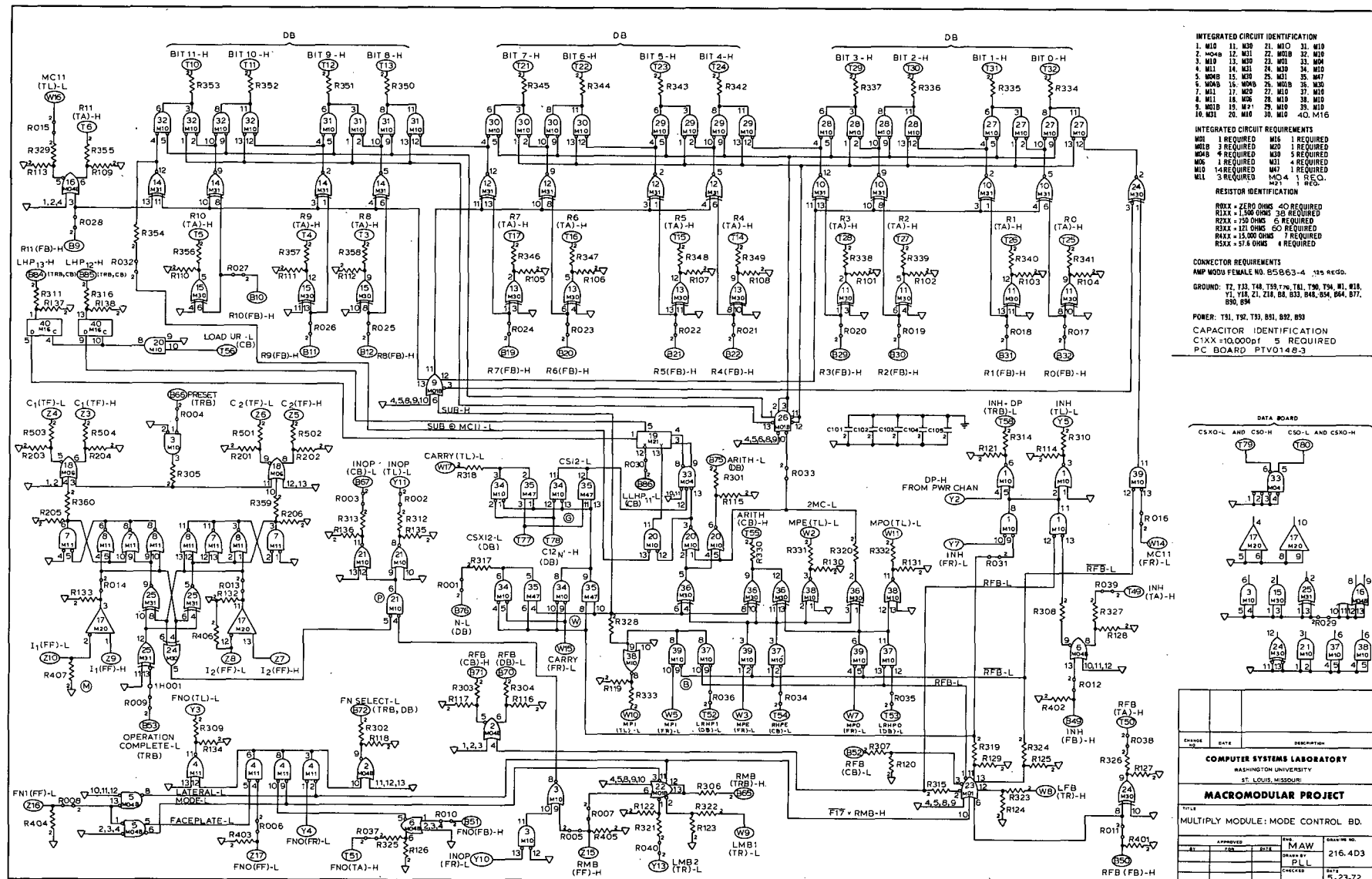
PTV0153-

Power: TFP6, T93, T92, T91, B93, B92, B91

Ground: B94, B90, B82, B60, B58, B50, B31
B21, B1, BFP18, BFP1, TFP18, TFP1
T94, T1, TL18, TL1, BL18, BL1

[illegible]





INTEGRATED CIRCUIT IDENTIFICATION

1. M10 11. M30 21. M10 31. M10
2. M04 12. M31 22. M08 32. M10
3. M10 13. M30 23. M03 33. M04
4. M11 14. M31 24. M30 34. M10
5. M08 15. M30 25. M31 35. M07
6. M08 16. M30 26. M08 36. M30
7. M11 17. M30 27. M10 37. M10
8. M11 18. M30 28. M10 38. M10
9. M08 19. M31 29. M10 39. M10
10. M31 20. M10 30. M10 40. M10

INTEGRATED CIRCUIT REQUIREMENTS

M10 1 REQUIRED M16 1 REQUIRED
M18 3 REQUIRED M20 1 REQUIRED
M24 4 REQUIRED M29 5 REQUIRED
M36 1 REQUIRED M31 4 REQUIRED
M10 14 REQUIRED M37 1 REQUIRED
M11 3 REQUIRED M44 1 REQ.
M21

RESISTOR IDENTIFICATION

R1XX - ZERO OHMS 40 REQUIRED
R1XX - 1.50 OHMS 35 REQUIRED
R2XX - 750 OHMS 6 REQUIRED
R3XX - 12 OHMS 50 REQUIRED
R4XX - 15.00 OHMS 7 REQUIRED
R5XX - 57.6 OHMS 4 REQUIRED

CONNECTOR REQUIREMENTS

AMP MODU FEMALE NO. 85B63-4 .155 reqd.
GROUND: T2, T33, T4, T33, T4, T40, T34, M1, M18,
V1, V18, Z1, Z18, B8, B33, B48, B54, B64, B77,
B90, B94

POWER: T31, T32, T33, B31, B32, B33

CAPACITOR IDENTIFICATION
C1XX - 10.000PF 5 REQUIRED
PC BOARD - PTV0146-3

DATA BOARD

CSX0-L AND CS0-H CS0-L AND CSX0-H

CSX0-L AND CS0-H CS0-L AND CSX0-H

CSX0-L AND CS0-H CS0-L AND CSX0-H

CSX0-L AND CS0-H CS0-L AND CSX0-H

CSX0-L AND CS0-H CS0-L AND CSX0-H

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CSX0-L AND CS0-H CS0-L AND CSX0-H

COMPUTER SYSTEMS LABORATORY

WASHINGTON UNIVERSITY
ST. LOUIS, MISSOURI

MACROMODULAR PROJECT

TITLE: MULTIPLY MODULE: MODE CONTROL BD.

APPROVED: DATE: 5.23.72

APPROVED: DATE: 5.23.72

APPROVED: DATE: 5.23.72

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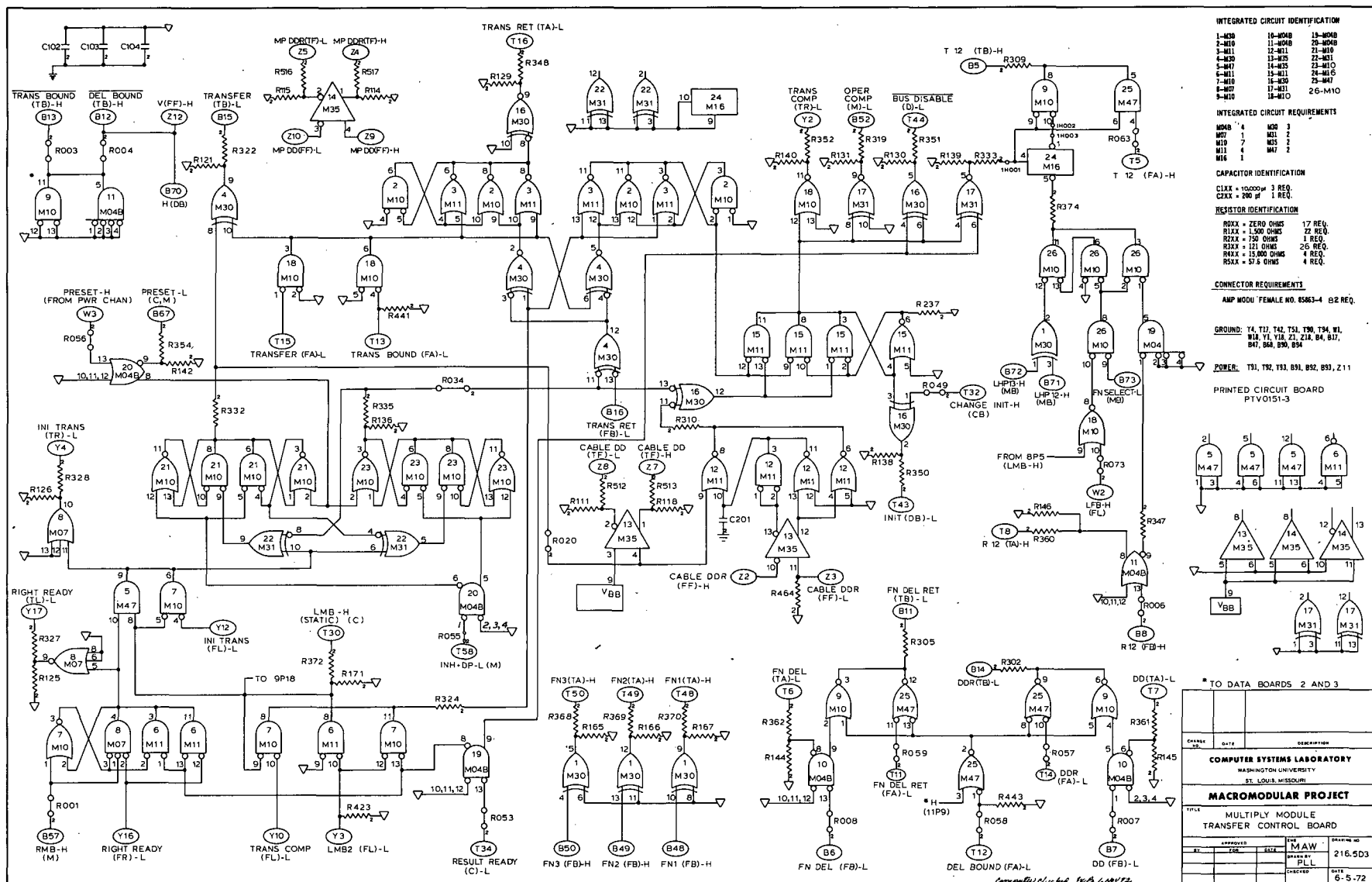
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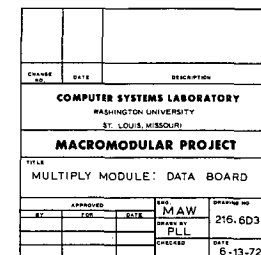
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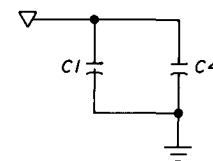
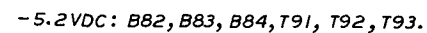
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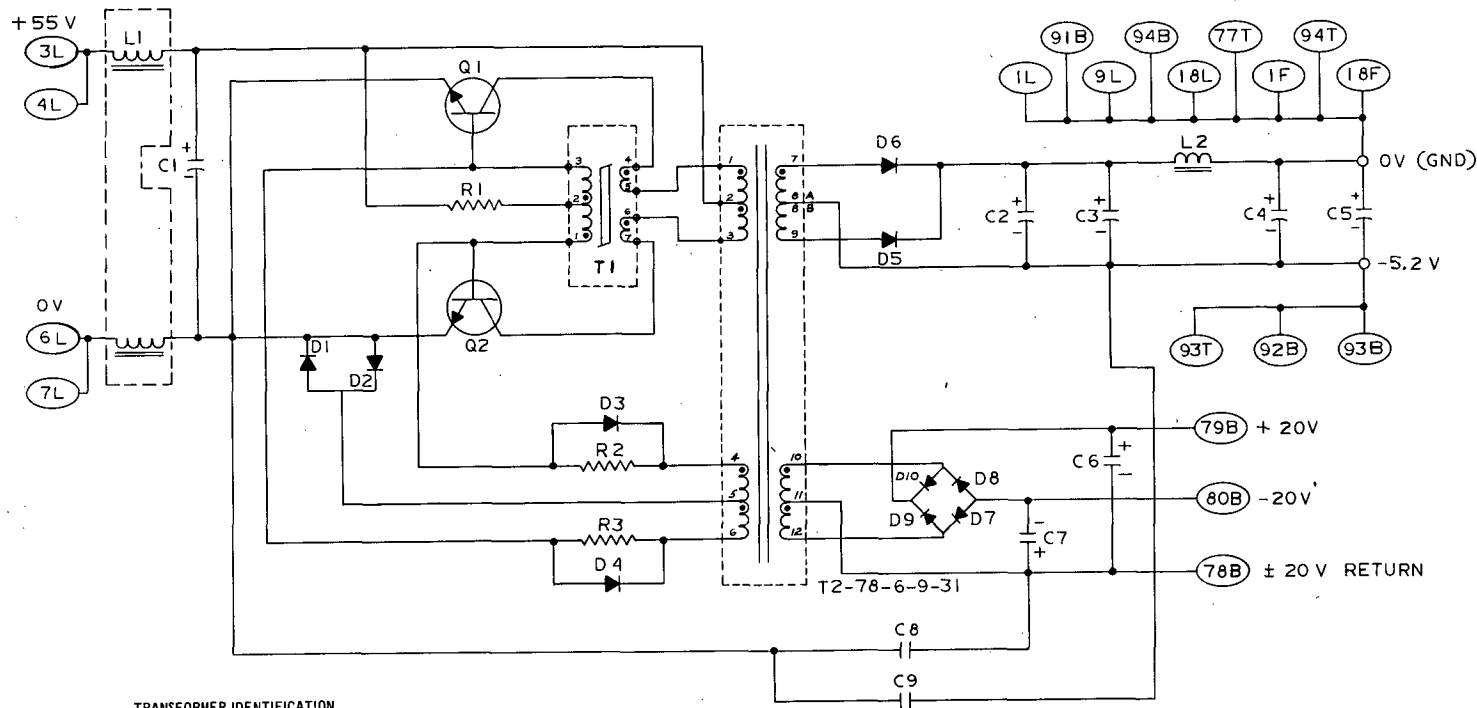


CHARGE TO		DATE		DESCRIPTION	
COMPUTER SYSTEMS LABORATORY					
WASHINGTON UNIVERSITY					
ST. LOUIS, MISSOURI					
MACROMODULAR PROJECT					
TITLE					
MULTIPLY MODULE					
TRANSFER CONTROL BOARD					
APPROVED				SIGN	EXPIRING ON
BY	DATE	DATE	DATE	MAW	216.503
				PLL	
				CHECKED	DATE 6-5-72





CHANGE NO.	DATE	DESCRIPTION
<p align="center">COMPUTER SYSTEMS LABORATORY.</p> <p align="center">WASHINGTON UNIVERSITY</p> <p align="center">ST. LOUIS, MISSOURI</p>		
<p align="center">MACROMODULAR PROJECT</p>		
<p>TITLE POWER SUPPLY SCHEMATIC MULTIPLY AND GMC MODULES</p>		
APPROVED		ENO.
BY	FOR	DATE
DRAWN BY		DRAWING NO.
P.L.L.		216.1203
CHECKED		DATE
T.B.C.		2-16-74



TRANSFORMER IDENTIFICATION

T1 = MPS-T1
T2 = MPS-T2 -78-6-9-31

INDUCTOR IDENTIFICATION

L1 = MPS-L3
L2 = MPS-L2

TRANSISTOR REQUIREMENTS

Q1, Q2 = RCA 40374

DIODE REQUIREMENTS

D1, D2, D3, D4, D7, D8, D9, D10 = MOTOROLA MR810
D5, D6 = MOTOROLA SR1922A

CAPACITOR REQUIREMENTS

C1 = 25 μ F 60V
C2, C3, C4, C5 = 4.7 μ F 50V
C5, C8, C9 = .47 μ F 12V

RESISTOR REQUIREMENTS

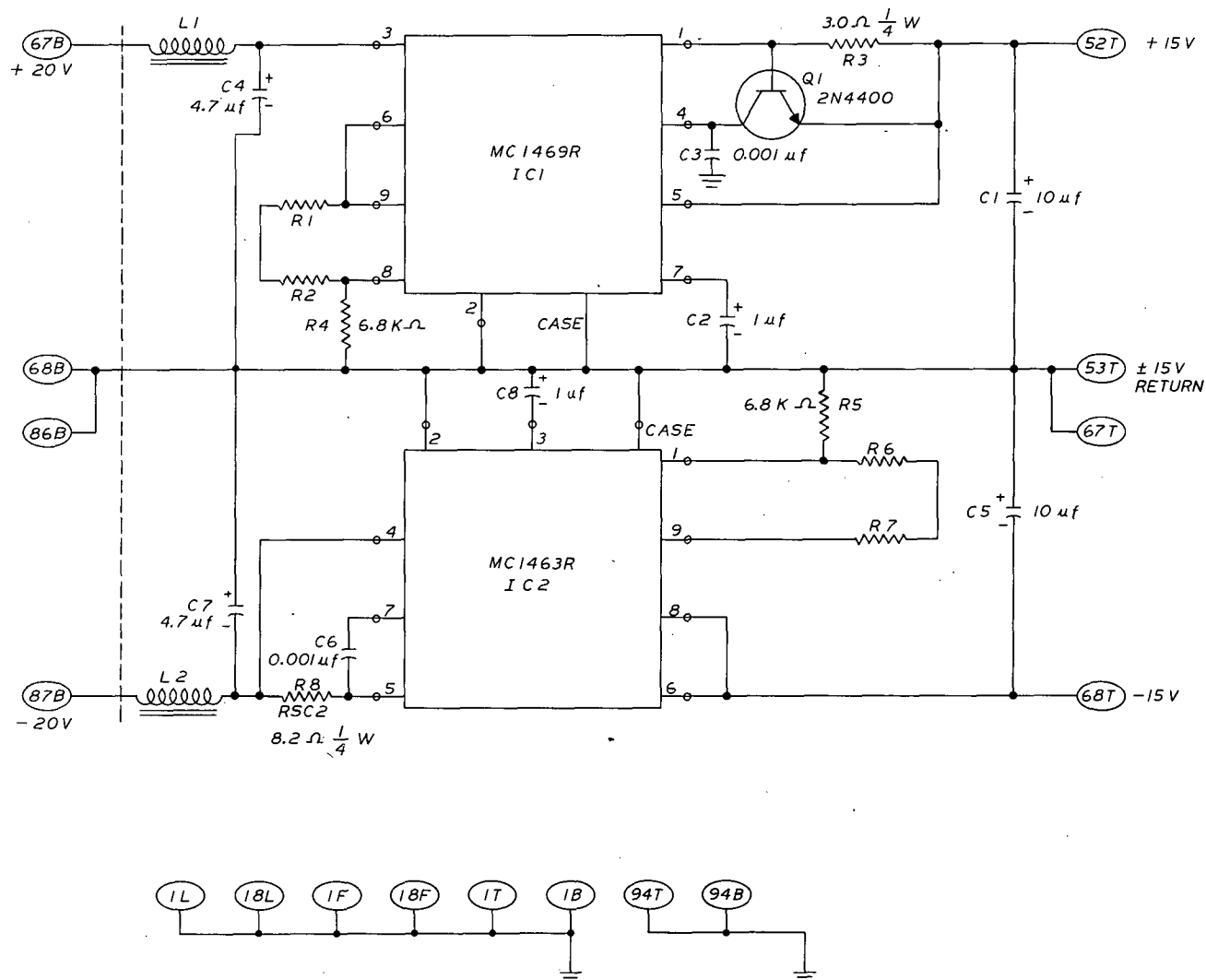
R1 = 13,000 OHMS $\frac{1}{4}$ W.
R2, R3 = 75 OHMS $\frac{1}{4}$ W.

CONNECTOR REQUIREMENTS

19 FEMALE

PRINTED CIRCUIT BOARD
PTV0117-1

CHANGE NO.	DATE	DESCRIPTION
COMPUTER SYSTEMS LABORATORY WASHINGTON UNIVERSITY ST. LOUIS, MISSOURI		
MACROMODULAR PROJECT		
TITLE 15 WATT DC DC 5 VOLT, \pm 20V CONVERTER SCHEMATIC PART NO 217.1		
APPROVED	ENG	DRAWING NO.
BY	FUR	217.1D3
FOR	DRAWN BY	
DATE	PLL	
CHECKED	DATE	
2UR	1-28-71	



RESISTOR IDENTIFICATION

R4, R5 = 6.8K OHMS
R1, R6 = RANGES SELECTED FROM 100 OHMS TO 2000 OHMS
R2, R7 = 20K OHMS; 22.1K OHMS OR 23.7K OHMS
R3 = 3.0 OHMS
R8 = 8.2 OHMS

COILS REQUIRED

L1, L2 = MPS-L2

SERIES REGULATOR

IC1 = MC1469R

IC2 = MC1463R

TRANSISTOR REQUIRED

Q1 = 2N4400

CAPACITOR REQUIREMENTS

C1 & C5 10µf 20V

C2 & C8 1µf 35V

C3 & C6 .001µf

C4 & C7 4.7µf 50V

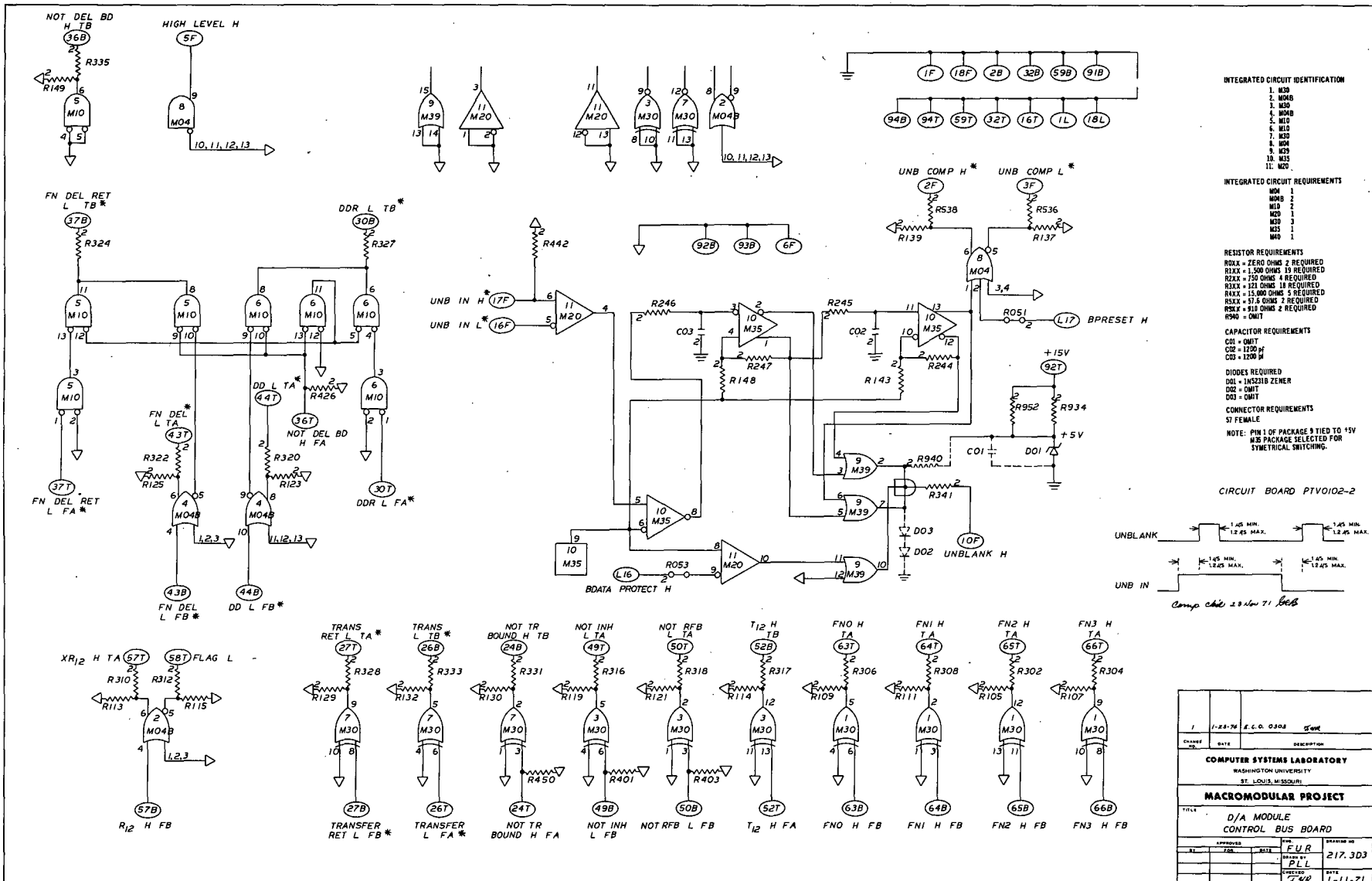
CONNECTOR REQUIREMENTS

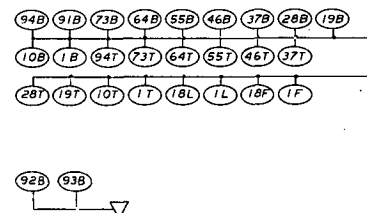
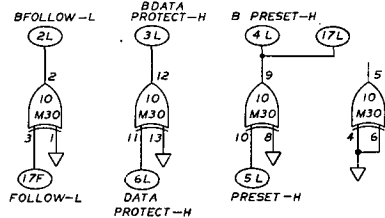
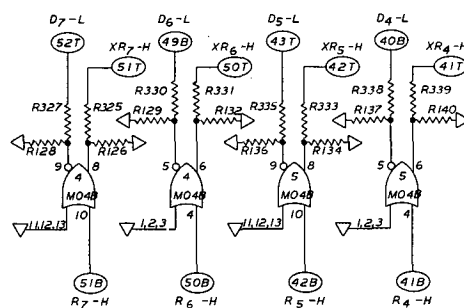
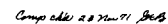
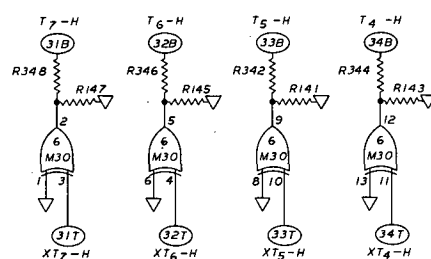
16 FEMALE

CIRCUIT BOARD

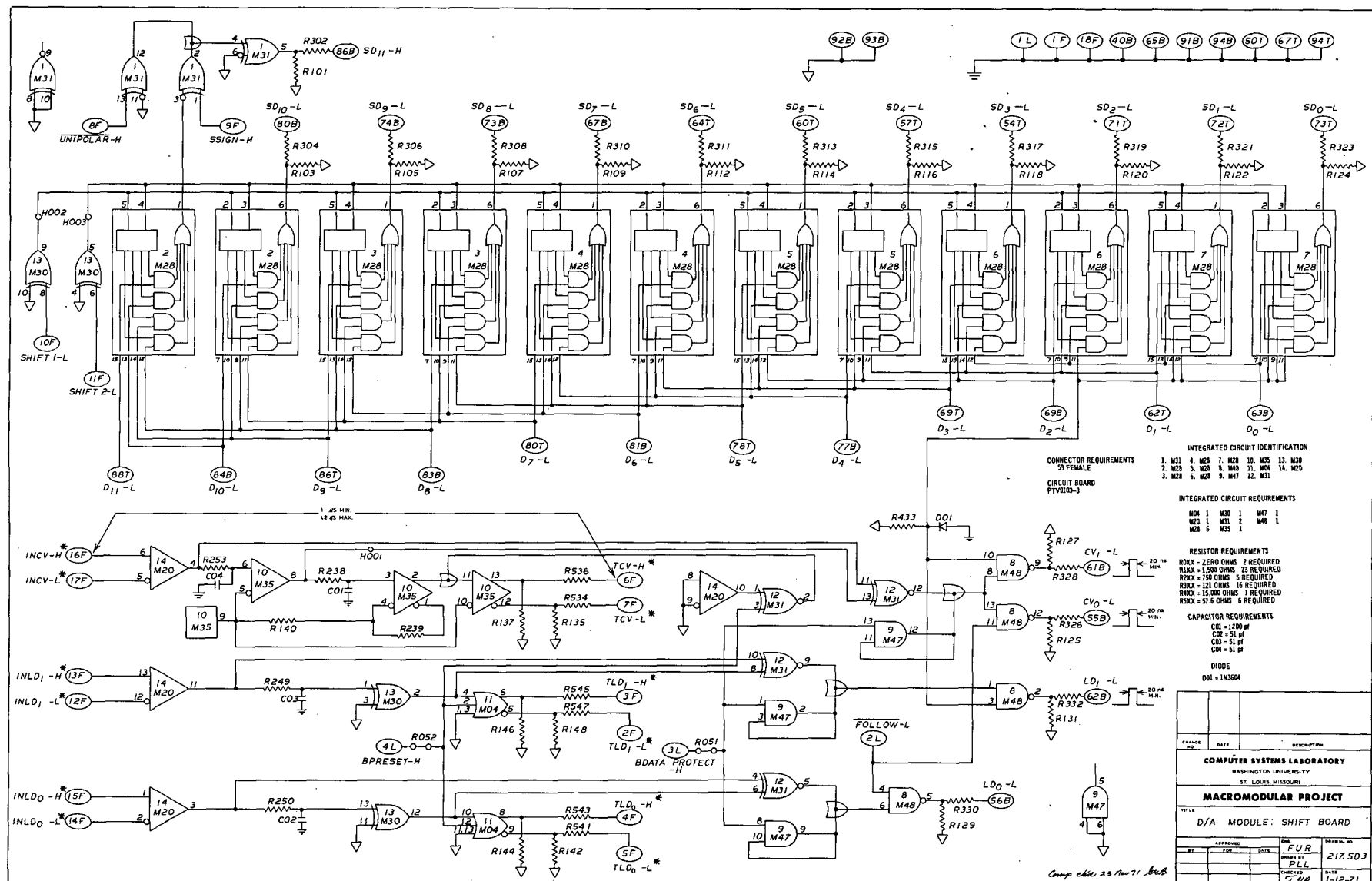
PTV0118-1

CHANGE NO.	DATE	DESCRIPTION
<p align="center">COMPUTER SYSTEMS LABORATORY WASHINGTON UNIVERSITY ST. LOUIS, MISSOURI</p>		
<p align="center">MACROMODULAR PROJECT</p>		
<p>TITLE CIRCUIT DIAGRAM SERIES REGULATOR PART NO. 2172</p>		
APPROVED	ENG.	DRAWING NO.
BY	FUR	217.2D3
FOR	DATE	
DRAWN BY	PLL	
CHECKED	DATE	
24R	1-22-71	





COPIES TO	DATE	DESCRIPTION	
<p align="center">COMPUTER SYSTEMS LABORATORY WASHINGTON UNIVERSITY ST. LOUIS, MISSOURI</p>			
<p align="center">MACROMODULAR PROJECT</p>			
TITLE <p align="center">D/A MODULE: BUS BOARD PART NO. 217.4</p>			
APPROVED		SIG.	ISSUED NO.
BY	DATE	FUR	217.403
C.T.	F.M.	P.L.	
		ENCLAVE	DATE
		258	1-19-70



INTEGRATED CIRCUIT IDENTIFICATION

CONNECTOR REQUIREMENTS
59 FEMALE
CIRCUIT BOARD
PTV003-3

INTEGRATED CIRCUIT REQUIREMENTS

M04 1 M30 1 M47 1
M05 1 M31 2 M48 1
M06 1 M32 1 M49 1

RESISTOR REQUIREMENTS

R01X = 220 OHMS 2 REQUIRED
R1XX = 1.50K OHMS 23 REQUIRED
R2XX = 750 OHMS 5 REQUIRED
R3XX = 12K OHMS 16 REQUIRED
R4XX = 15.00K OHMS 1 REQUIRED
R5XX = 51.5 OHMS 6 REQUIRED

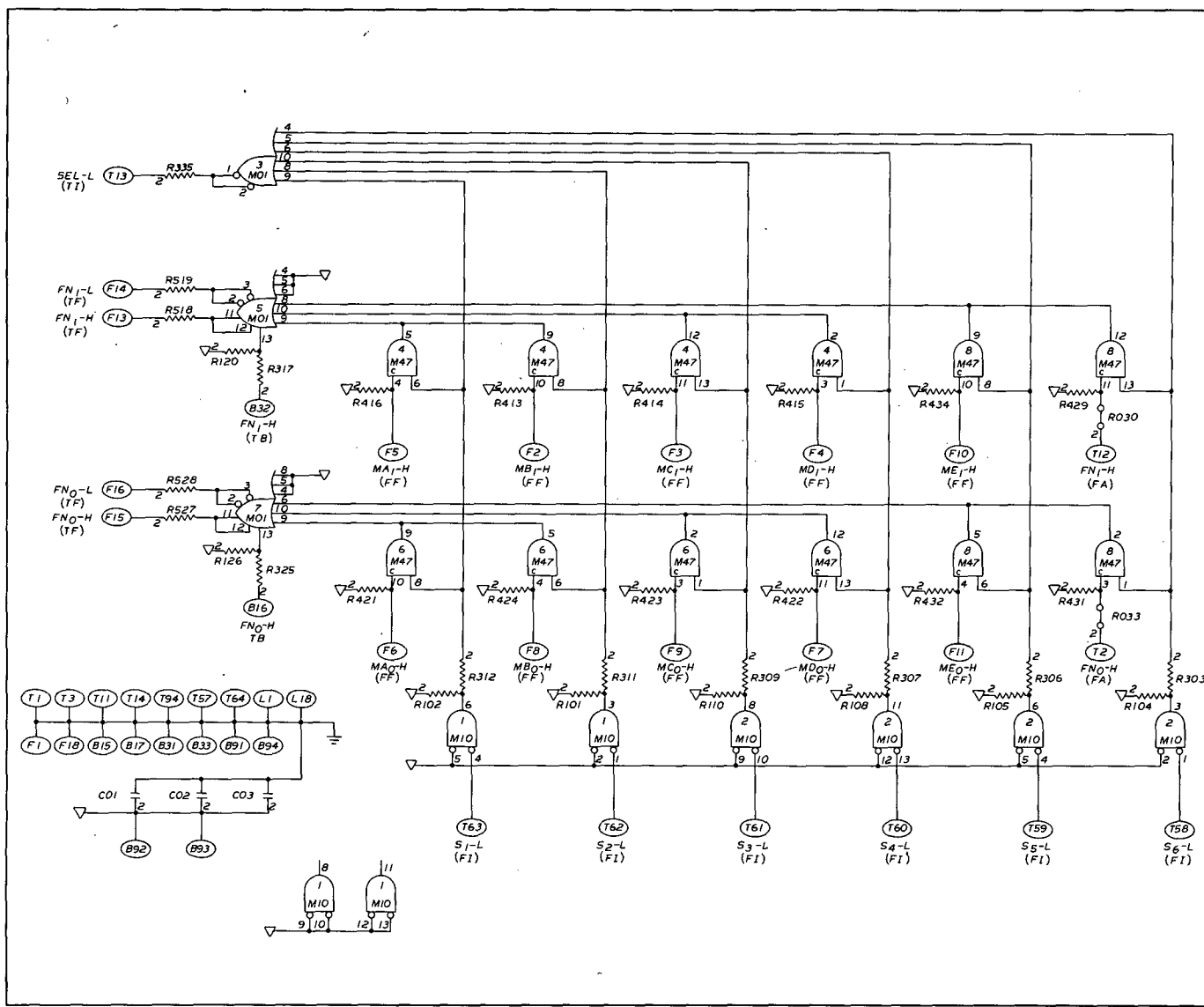
CAPACITOR REQUIREMENTS

C01 = 1200 pF
C02 = 51 pF
C03 = 51 pF
C04 = 51 pF

DIODE

D01 = 1N3504

CHANGE NO.	DATE	DESCRIPTION
COMPUTER SYSTEMS LABORATORY		
WASHINGTON UNIVERSITY		
ST. LOUIS, MISSOURI		
MACROMODULAR PROJECT		
TITLE		
D/A MODULE: SHIFT BOARD		
APPROVED	DATE	DESIGN NO.
BY	FOR	217.503
PL		
DATE		
1-12-71		



INTEGRATED CIRCUIT IDENTIFICATION

1-M10
2-M10
3-M01
4-M47
5-M01
6-M47
7-M01
8-M47

INTEGRATED CIRCUIT REQUIREMENTS

M01 3
M10 2
M47 3

RESISTOR IDENTIFICATION

R0XX = ZERO OHMS 2 REQ.
R1XX = 1500 OHMS 4 REQ.
R2XX = 121 OHMS 9 REQ.
R4XX = 15000 OHMS 12 REQ.
R5XX = 57.6 OHMS 4 REQ.

CAPACITOR IDENTIFICATION

CO1 = 0.1 uF
CO2 = 0.1 uF
CO3 = 0.1 uF

CONNECTOR REQUIREMENTS

AMP MODU FEMALE NO. 8563-4 44 REQ.

PRINTED CIRCUIT BOARD PTV 0136-1

CHANGE NO.	DATE	DESCRIPTION
<p>COMPUTER SYSTEMS LABORATORY WASHINGTON UNIVERSITY ST. LOUIS, MISSOURI</p>		
<p>MACROMODULAR PROJECT</p>		
<p>FUNCTION CALLER MULTIPLEXER BOARD</p>		
APPROVED	DATE	DESIGNER NO.
BY: [Signature]	DATE: [Date]	218.403
CHECKED	DATE	
DATE: 2-28-72		

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