Macromodular Computer Design, Part 2, Volume 05, Logic Drawings

Computer Systems Laboratory, Washington University

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MACROMODULAR
COMPUTER DESIGN
PART 2
MANUFACTURING DESCRIPTION

VOLUME V
LOGIC DRAWINGS

Technical Report No. 34

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COMPUTER SYSTEMS LABORATORY
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ABSTRACT

This volume contains the circuit diagrams for the vertical boards used in the macromodule electronic subassemblies.
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A GUIDE TO DRAWING CONVENTIONS

In the process of designing a circuit board, the logic drawing has been our principal piece of documentation up until the time that the production documents are generated. The drawings thus contain circuit diagrams, parts lists, component counts, and certain information that is useful at specific stages of the design process. About half of the drawings in this volume are original logic drawings. The other drawings are revisions that no longer contain obsolete information or information to be found elsewhere. The revisions also have an improved notational form. In the text that follows, we first treat the conventions common to all of the drawings in this volume, and then treat the conventions peculiar to specific subsets of the drawings.

1. LOGIC FUNCTION SYMBOLOGY

The logic function symbology conforms in general to MIL-STD-806B. The principal exceptions are as follow:

A) **Function Identification**  Only two tagging lines are used. The top line locates the function on the circuit board and the bottom line identifies the hardware. Most logic hardware used in the modules is Motorola's MECL II series. This logic hardware is identified by an M followed by two digits. The M is an abbreviation for MC12 so that a tag such as M47 identifies the element as an MC1247. When there is also a letter suffix, e.g. M47B, the suffix indicates that the hardware is tested to standards other than those specified by Motorola. For more information on that, see the section on IC Testing. When hardware is not MECL II series, the bottom tag line contains the manufacturer's own designation number.
B) Interconnected Outputs  The outputs of MECL II circuits can be tied together to implement the AND and OR functions, a feature which has been used extensively in the design of the modules. When outputs are tied together, the interconnection point is high if one or more of the outputs are high (the OR function) and is low if all outputs are low (the AND function). In the circuit diagrams, the interconnection point is generally not enveloped by a logic symbol. The symbols have been omitted in order to reduce the overall density of logic symbols and thereby make the drawings easier to read.

2. OTHER CONVENTIONS --- ALL DRAWINGS

A) The symbols used for components such as resistors, capacitors, diodes, etc., are industry standards. Each of these items is identified by a single tag line. In most cases, one must refer to the parts list for the circuit board in order to get any information about these components. This is only partly true for resistors, however. Resistors are tagged by an R followed by three digits. If the digit immediately following the R is listed in the table below, then the value of the resistor can be found from the table. If the digit is not in the table, then one must refer to the parts list.

<table>
<thead>
<tr>
<th>Digit</th>
<th>Resistor Value In Ohms</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>zero (a jumper)</td>
</tr>
<tr>
<td>1</td>
<td>1500</td>
</tr>
<tr>
<td>2</td>
<td>750</td>
</tr>
<tr>
<td>3</td>
<td>121</td>
</tr>
<tr>
<td>4</td>
<td>15K</td>
</tr>
<tr>
<td>5</td>
<td>57.6</td>
</tr>
<tr>
<td>6</td>
<td>130</td>
</tr>
</tbody>
</table>
B) Connector terminals for signals entering and leaving the circuit board are represented by ovals. Tags internal to the ovals identify the terminals.

C) A small triangle with no internal tag represents a connection to -5.2 volts. This voltage is $V_{EE}$ for MECL II circuits.

D) When MECL II logic functions are shown with inputs tied to -5.2 volts, the device behaves as if those inputs were tied to a logic low.

E) On some circuit boards, a few of the integrated circuits have unused logic elements. These elements are shown on the diagrams in a group unto themselves.

3. DRAWINGS 200.9D3 THROUGH 210.2D3

These are revisions of the original logic drawings. Obsolete information and information now found elsewhere has been eliminated. The circuit diagrams have been revised in an attempt to make them easier to understand and follow. They have the following features:

A) The elements of the diagram are arranged so as to minimize the number of long lines, minimize the number of interconnecting lines, and accentuate functional groupings. In a few instances, tie-points are used to eliminate long lines that could not be comfortably eliminated by other means. See 3D for an explanation of tie-point notation.

B) Certain functional groupings are enclosed in boxes and labeled to indicate the functions performed by the groupings.

C) Signals entering and leaving the circuit board are identified by two tag lines. One tag gives the name of the signal while the other tag, always in parentheses, indicates the significance of a logic high or low. (See 3E for a special case.) The polarity-indicating tag is subject to the following rules:
1. If the signal is a data bit, the polarity representing the data value 1 is indicated. The possible tags are (1-L) and (1-H).

2. If the signal is a condition, the polarity representing assertion of the condition is indicated. The possible tags are (A-L) and (A-H).

3. If the signal is a transition signal, the preset polarity of the signal is indicated. The possible tags are (P-L) and (P-H).

D) Two forms of tie-point notation have been used. The more commonly occurring form employs a triangle (flag) containing a letter tag. The rule is that all identically flagged points on a diagram are interconnected. The other form of tie-point notation occurs only on drawing 203.2D3. A tie-point source is identified by a small arrow which is usually perpendicular to a line and pointing away from it. The number of destinations is indicated by a digit near the arrow. If the line to which the arrow is affixed is not already named, a name is given at the head of the arrow. A tie-point destination is identified by a logic function input connected to a tag. This tag is either the signal name of the tie-point source or the complement (NOT) of it. The assertion polarity (or value 1 polarity) for this tag agrees with the assertion polarity of the input to which it is connected.

E) On drawings 205.2D3 and 210.2D3 there is a pair of inputs whose second tagging line is "(A-NC)." The possible states for these inputs are NC (no connection) and ground (zero volts).
4. DRAWINGS 211.3D3 THROUGH 218.4D3

A) A small circle on a line (with a tag beginning with an H or a 1H) specifies a plated-through-hole into which a component is not inserted. The function of this hole is to take the signal from one surface of the circuit board to the other surface. This type of information has been deleted on the revised drawings discussed in section 3.

B) The numbers 1 and 2 that occur at the ends of resistors, capacitors, and diodes are engineering aids that were useful at a specific phase of the circuit board design process. These numbers should be ignored.

C) The character string that identifies a signal entering (or leaving) a circuit board can be considered a single tag. Somewhere within this tag there is either an isolated L or H, or there is a -L or a -H. These are the polarity indicators. The significance of the indicator depends on the nature of the signal, i.e., depends on whether the signal is a data bit, a condition, or a transition signal. For modules other than the Multiply and Interlock modules, an asterisk identifies the signal as a transition signal and the polarity indicator thus indicates the preset polarity for the signal. Except for this, the nature of the signal is not indicated in the tag.
THE TURNS RATIO OF T2 IS MATCHED TO THE LOAD OF THE TYPE MODULE IN WHICH IT WILL BE USED.

GND: T52, T61, T94, F1, F18, L1, L6, L18, B51, B52, B91, B94.
-5.2V: B92, B93, T93.
TEST COMPLETE (P-L)

TEST COMPLETE (P-L)

DUAL DELAY

CR

DELAY

BEGIN DELAY

COMPARISON MODULE

TRANSFER CONTROL BOARD

GNDs: 158, 159, 172, 176, 190, 194, L1, L15, F1, F10, 895, 899, 901, 904.

Vee: 992, 993.
NOTE: FN, XFN, AND CODE DRIVER HAVE NO FUNCTION IN THE PRESENT INTERLOCK MACROMODULE.
GNDS: T1, T2, T37, T38, T39, T40, T69, T70, T91, T90, T94, B1, B2, B19, B20, B69, B70, B81, B85, FBI, F818, LT1, LT9, LT14, LT18, LBI, LBI8, B94.

- 5.2 VDC: B82, B83, B84, T91, T92, T93.
This volume contains the circuit diagrams for the vertical boards used in the macromodule electronic subassemblies.
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